REDUCTION OF CAPACITOR RIPPLE VOLTAGE AND CURRENT WITH FUZZY CONTROL IN MODULAR MULTILEVEL CONVERTER BASED VARIABLE SPEED DRIVES

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Abstract—In this paper**,** The major drawback of Modular Multilevel Converter (MMC) based variable speed drives is that the capacitor voltage ripple varies inversely with the output frequency. This voltage ripple can be reduced at lower operating frequency by injecting circulating current into its each arm using fuzzy logic. However, this circulating current increases the overall current rating of the converter. The voltage ripple can also be reduced by reducing the dc bus voltage when the drive is required to be operated at lower speeds. In this paper, a new configuration using multipulse diode bridge rectifier is proposed to reduce the dc bus voltage when the drive is operated at lower speeds with fuzzy logic. Therefore, the capacitor ripple voltage is reduced without injecting any circulating current. The proposed configuration is simulated in MATLAB/Simulink and the simulation results are presented to validate the proposed configuration.

Keywords—Medium voltage drives, Modular multilevel converter, Multipulse rectifier, Variable Speed Drives, fuzzy.

I. INTRODUCTION TO MMC

Multilevel converters have gained popularity in high power applications due to their advantages such as low device switching frequency, lower voltage steps and reduced filter requirement.[1] Modular Multilevel Converter (MMC) is the most recent development in multilevel converter family which was originally proposed for high voltage dc transmission system.[2] The power circuit of a three phase MMC is shown in Fig. 1, which has three legs with two arms per leg. Each arm consists of N number of series connected sub modules (SM) and an inductor. The configuration of half bridge sub module (HB-SM) and full bridge sub module (FB-SM) are shown in Figs. 1(b) and 1(c) respectively. Due to its simple and modular structure, research is being done to use it as a possible solution for medium voltage high power variable speed ac drives[3],[4]. However, the major drawback of MMC based drives is that it suffers from SM capacitor voltage fluctuation at low speeds as its peak to peak value is inversely proportional to the output frequency[5]. This becomes severe particularly for constant torque loads.

The capacitor voltage ripple can be reduced by injecting higher frequency circulating current and common mode voltage into each arm of the converter[6]. This additional circulating current increases the current rating of the switching devices, arm inductors and capacitors. The arm current rating could be as high as three times than that is required at rated torque and speed to achieve constant torque over the whole speed range.

Various improved circulating current injection methods like square wave, hybrid injection method are proposed in the literature to reduce the peak value of the arm current[7]. However, the arm current is still more than that is required to produce the rated torque at rated speed. Moreover, the higher frequency common mode voltage is critical for drives system as it forces bearing current which may lead to its premature failure. Therefore, it remains a challenge to operate the drive at constant output torque for whole speed range. The use of variable dc bus voltage is proposed to reduce the capacitor voltage ripple for variable speed drives[5],[6].

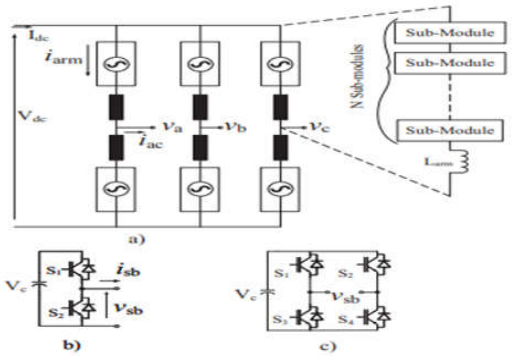


Fig.1: Circuit configuration of a modular multilevel converter. a) Three phase converter, b) half bridge submodule, c) full bridge submodule.

Reduction of dc bus voltage at lower output frequency also reduces the capacitor ripple current compared to the constant dc bus voltage operation. Active front end (AFE) rectifier with FB-SM based MMC is one possible solution to vary the dc bus voltage, which has the advantage of regenerating

power back to the grid. However, if the regeneration mode of operation is not required, the dc bus is normally supplied by multipulse diode bridge rectifiers along with phase shifting transformer to eliminate the lower order harmonic components from the source current. The idea of buck converter is used as intermediate converter to reduce the average dc bus voltage of the MMC. However, the input side current is discontinuous, which requires additional filter circuit at the input side. Moreover, the intermediate converter reduces the overall reliability of the drive system.

II MULTILEVEL CONVERTER DESIGN

In a multilevel inverter, determining the number of levels will be one of the most important factors because this affects many of the other sizing factors and control techniques[6]. Trade offs in specifying the number of levels that the power conditioner will need and the advantages and complexity of having multiple voltage levels available are the primary differences that set a multilevel filter apart from a single level filter.

As a starting point, known is the nominal RMS voltage rating, V_{nom}; of the electrical system to which the diode clamped power conditioner will be connected. The parallel inverter must be able to inject currents by imposing a voltage across the parallel inductors, L_{PI}, that is the difference between the load voltage V_L and parallel inverter output voltage V_{PI}. Without this margin, complete compensation of reactive currents may not be possible[7]. This margin can be incorporated into a design factor for the inverter. Because the DC link voltage and the voltage at the connection point can both vary, the design factor used in the rating selection process incorporates these elements as well as the small voltage drops that occur in the inverters during active device conduction. The minimum number of levels and the voltage rating of the active devices (IGBTs, GTOs, power MOSFETs, etc.) are inversely related to each other. More levels in the inverter will lower the required voltage device rating of individual devices or looking at it another way, a higher voltage rating of the devices will enable a fewer minimum number of levels to be used.

1. Voltage stress across each device is lower. Both active devices and DC link capacitors could be used that have lower voltage ratings (which sometimes are much cheaper and have greater availability).
2. The inverter will have a lower EMI because the dV/dt during each switching will be lower.
3. The output of the waveform will have more steps, or degree of freedom, which enables the output waveform to more closely track a reference waveform.
4. Lower individual device switching frequency will achieve the same results as an inverter with a fewer number of levels and higher device switching frequency[8]. Or the switching frequency can be kept the same as that in an inverter with a fewer number of levels to achieve a better waveform.

The drawbacks of using more than the required minimum number of levels are as follows:

1. Six active device control signals (one for each phase of the parallel inverter and the series inverter) are needed for each hardware level of the inverter i.e., 6□(m-1) control signals. Additional levels require more computational resources and add complexity to the control.
2. If the blocking diodes used in the inverter have the same rating as the active devices, their number increases dramatically because 6□(m-2)□(m-1) diodes would be required for the back to back structure.

III MMC IN VARIABLE SPEEED DRIVES

In MMC, the current and voltage of each SM in the upper arm of phase-a are,

$$i_{sb} = \frac{I_{dc}}{3} + \frac{\hat{I}_{ac}}{2}\sin(\omega_0 t - \phi) \quad (1)$$

$$v_{sb} = \frac{V_c}{2} - \frac{m V_c}{2}\sin(\omega_0 t), \quad (2)$$

where, m is the output voltage modulation index. In variable speed drives with constant torque load, m varies almost linearly with the output frequency[9]. Therefore, the modulation index and output frequency in per unit are used interchangeably in this paper.

Assuming the semiconductor devices are lossless, the peak to peak voltage ripple and rms value of the ripple current of the SM capacitor can be calculated as[2],[12] ,

$$\Delta V_c = \frac{2K_1}{\cos\phi}\frac{1}{m}\left[1 - \left(\frac{m\cos\phi}{2}\right)^2\right]^{3/2} \quad (3)$$

$$I_{crms} = \hat{I}_{ac}\frac{1}{4}\sqrt{\left(1 - \frac{m^2\cos^2\phi}{2}\right)}. \quad (4)$$

where K1 is constant for constant torque output at different speeds. It is evident that both the capacitor ripple voltage and current increase when the

modulation index decreases[12]. However, with the variable dc bus voltage, these can be reduced which is evident from the following equations

$$\Delta V_c = \frac{2K_1}{\cos\phi}\frac{k}{m}\left[1-\left(\frac{m\cos\phi}{2k}\right)^2\right]^{3/2} \quad (5)$$

$$I_{crms} = \hat{I}_{ac}\frac{1}{4}\sqrt{k\left(1-\frac{m^2\cos^2\phi}{2k^2}\right)}. \quad (6)$$

Here, k represents the fraction of rated dc bus voltage and should always be more than or equal to modulation index in case of HB-SM based MMC. In MMC, the change of dc bus voltage is possible as RC filter with small capacitor is normally connected to the dc bus[17]. The dc bus voltage can be varied by using thyristorized bridge rectifier.

IV BUCK CONVERTER

In this circuit the transistor turning ON will put voltage V_{in} on one end of the inductor. This voltage will tend to cause the inductor current to rise. When the transistor is OFF, the current will continue flowing through the inductor but now flowing through the diode[10]. We initially assume that the current through the inductor does not reach zero, thus the voltage at V_x will now be only the voltage across the conducting diode during the full OFF time.

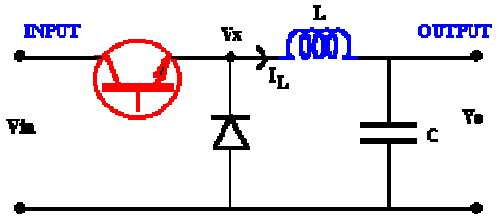


Fig.2. Buck Converter

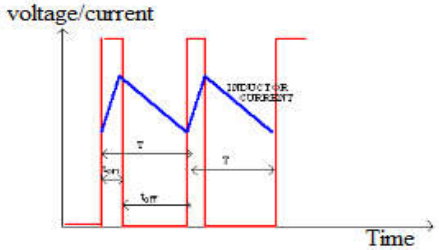


Fig.3. Voltage and current changes

To analyze the voltages of this circuit let us consider the changes in the inductor current over one cycle.
From the relation

$$V_x - V_o = L\frac{di}{dt} \quad \ldots(7)$$

the change of current satisfies

$$di = \int_{ON}(V_x - V_o)dt + \int_{OFF}(V_z - V_o)dt \quad \ldots(8)$$

For steady state operation the current at the start and end of a period T will not change. To get a simple relation between voltages we assume no voltage drop across transistor or diode while ON and a perfect switch change. Thus during the ON time $V_x=V_{in}$ and in the OFF $V_x=0$. Thus

$$0 = di = \int_0^{t_{on}}(Vin - Vo)dt + \int_{t_{on}}^{t_{on}+t_{off}}(-Vo)dt \quad \ldots. (9)$$

This simplifies to

$$(Vin - Vo)t_{on} - Vo\,t_{off} = 0 \quad \ldots (10)$$

or

$$\frac{Vo}{Vin} = \frac{t_{on}}{T} \quad \ldots (11)$$

and defining "duty ratio" as

$$D = \frac{t_{on}}{T} \quad \ldots. (12)$$

The voltage relationship becomes Vo=D Vin Since the circuit is lossless and the input and output powers must match on the average $V_o * I_o = V_{in} * I_{in}$. Thus the average input and output current must satisfy $I_{in} = D\, I_o$

V. PROPOSED CONFIGURATION

A. *Circuit configuration*

The dc bus is normally supplied by multipulse diode bridge rectifiers in non-regenerative drives. The multipulse rectifier operation can be achieved either by connecting the diode bridge rectifiers in series or in parallel[15]Fig.4 shows the proposed circuit configuration for the 24-pulse rectifier based MMC drive, which allows the diode bridges to be connected either in series or in parallel. All the diode bridges are connected in series to

achieve the rated dc bus voltage, when the drive is operated near the rated output frequency.
The circuit arrangement allows the diode bridges to be connected in parallel to reduce the dc bus voltage to 50% and 25% of its rated value at lower output frequency. The connection between diode bridges for three possible values of the dc bus vol dc bus voltage

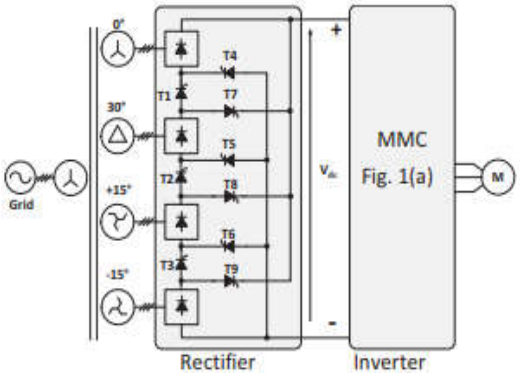


Fig.4. Proposed configuration of the MMC based drive

are shown in Fig 5. In case of HB-SM based MMC, the minimum dc bus voltage required is decided by the peak value of the output voltage. Therefore, to produce an output voltage higher than 0.5 pu, rated dc bus voltage is applied to the MMC. Similarly, half of the rated dc bus voltage is applied to generate output voltage between 0.25 pu to 0.50 pu. The dc bus voltage is reduced to 25% of its rated value when the output voltage is less than 0.25 pu.

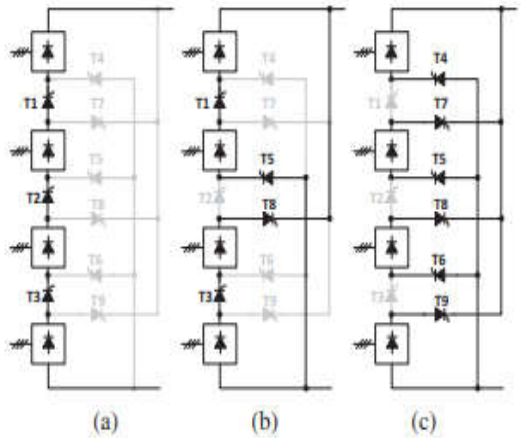


Fig.5.Different switching states of the rectifier for : a) rated dc bus voltage, b) 50% of rated dc bus voltage, c) 25% of rated dc bus voltage.

B. Selection of the switches

The switches T1-T3 need to block only forward voltage, whereas T4-T9 are required to block forward as well as reverse voltages. During the transition, the dc-link current is first reduced to zero to avoid the high voltage spike due to the arm inductance of MMC. Therefore, the switching losses of the devices are reduced. The voltage and current ratings of the switches (T1-T9) are given in Fig.6. The maximum voltage rating of the switches is 75% of the rated dc bus voltage, which appears across the device T4 and T9 when the rated dc bus voltage is applied. Similarly, the current ratings of the switches T1, T2 and T3 are maximum and equal to rated dc bus current[13],[14].

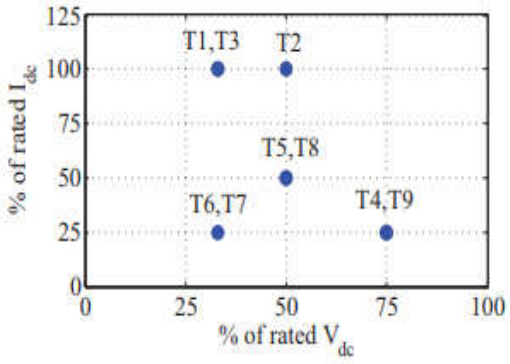


Fig.6. Voltage and current ratings of the switching devices.

C. Control scheme

Conventional control scheme[8]is used to control the voltage of all the SM capacitors. The block diagram of control technique is shown in Fig.7. The sum of all the SM capacitor voltages is maintained at its reference value by overall energy balancing controller, which generates the dc bus current reference,Iref dc of the MMC.The dc bus current is maintained at its reference value by dc current controller. The dc current controller generates the control voltage, vcntl of each leg. This control voltage is equally divided to the 2N number of SM of one leg. Second harmonic suppression technique is used to reduce the second harmonic component of arm current.

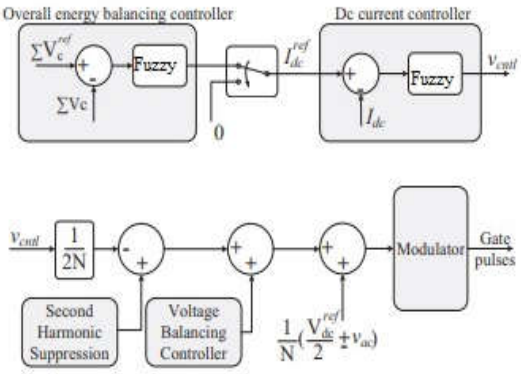


Fig.7 Block diagram of the control scheme.

The individual capacitor voltages are balanced by cluster voltage balancing and individual voltage balancing controller. All these voltage components along with dc voltage reference, V ref dc /2N and ac output voltage vac/N are added to generate the voltage reference for each SM[15]. These voltage references are modulated by phase shifted PWM technique to generate the gate pulses for the switches of each SM.

D.Change of dc bus voltage

The change of dc bus voltage is performed when the output voltage reaches some predefined values. During the transition, the dc bus current is first reduced to zero to avoid high voltage spike due to the arm inductance of MMC. The advantage of MMC is that the dc bus current can be made zero momentarily as SM capacitors can supply the output power during the transition. The average value of SM capacitor voltage drops but this is not more than 10% as this whole transition takes place in less than one cycle of the grid frequency.

The sequence of this process to make a smooth transition is summarized as follows:

1) The gate pulses from all the thyristors are blocked. However, to turn off the thyristor the dc bus current must be zero.

2) The dc bus current reference, Iref dc is made zero by bypassing the output of overall energy balance controller in Fig.5

3) Dc bus voltage reference, V ref dc in Fig.5 is changed in small steps towards the next desired dc bus voltage. This change in small steps is required to avoid high dv/dt across the dc bus filter capacitor.

IV.FUZZY LOGIC CONTROLLER

In recent years, the number and variety of applications of fuzzy logic have increased significantly. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision-support systems, and portfolio selection. To understand why use of fuzzy logic has grown, you must first understand what is meant by fuzzy logic

A.THE FIS EDITOR

The FIS Editor handles the high level issues for the system: How much input and output variables? What are their names? The Fuzzy Lo Tgicoolbox

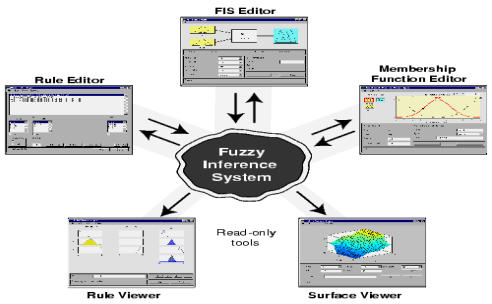


Fig.8 The Primary GUI Tools Of The Fuzzy Logic Toolbox

doesn't limit the number of inputs. However, the number of inputs may be limited by the available memory of your machine[12]. If the number of inputs is too large, or the number of membership functions is too big, then it may also be difficult to analyze the FIS using the other GUI tools.

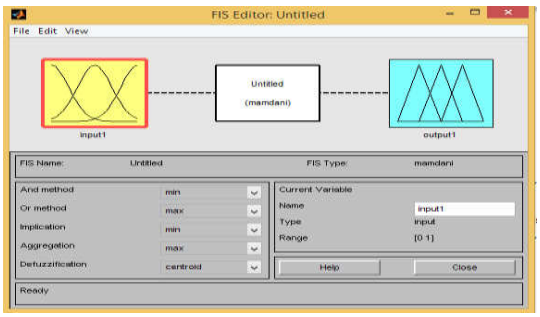


Fig.9 FIS Editor

By saving to the workspace with a new name, you also rename the entire system. Your window will look like as shown in Fig.10

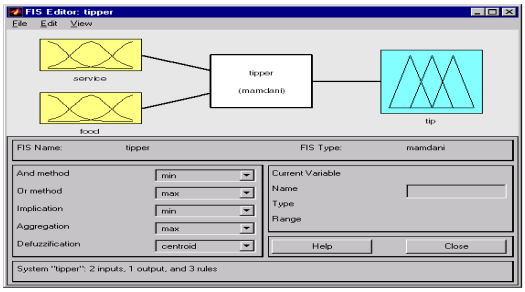


Fig.10 The updated FIS Editor

B. THE MEMBERSHIP FUNCTION EDITOR

The Membership Function Editor is used to define the shapes of all the membership functions associated with each variable. The Rule Editor is for editing the list of rules that defines the behavior of thesystem.

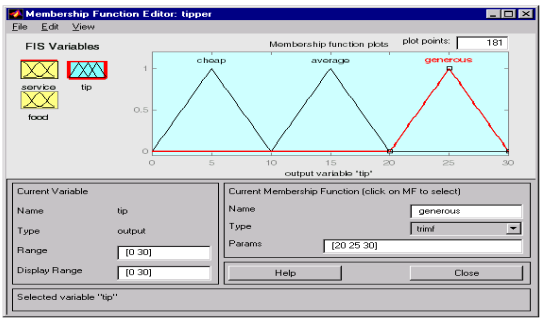


Fig.11 The Rule Editor

	NB	NS	PS	PB
NB	PB	PB	NB	NB
NS	PS	PS	NS	NS
PS	NS	NS	PS	PS
PB	NB	NB	PB	PB

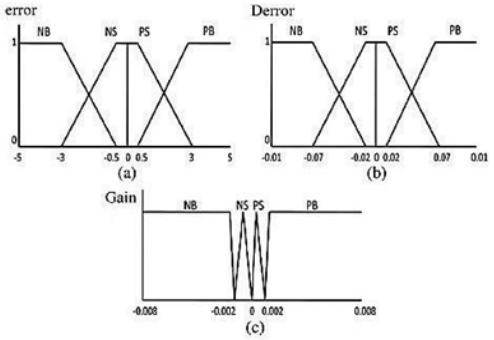


Fig.12: Fuzzy rules

VI. SIMULATION RESULTS

Simulation study on a 3.3 kV, 1 MW MMC drive system is carried out in MATLAB/Simulink with the parameters given in Table I. The rated dc bus voltage is considered as 5600 V to produce output line voltage of 3.0 kV. Considering 6% drop across the transformer leakage inductance at rated operating condition, the secondary to primary line to line voltage ratio is chosen as 1.3.

The capacitor voltage ripple at output frequency of 0.2 pu at rated torque with the rated dc bus voltage and 25% of the rated dc bus voltage are shown in Figs.15,16 and 17,18 respectively. There is a significant reduction in capacitor ripple voltage when the dc bus voltage is reduced. It is to be noted that at lower output frequency, the fundamental frequency component in the capacitor ripple voltage is dominant compared to the second harmonic component [19]. Fig 17 shows the comparison of arm currents between hybrid circulating current injection method [10] and reduced dc bus voltage method for the same amount of SM capacitor voltage ripple at output frequency of 0.2 pu and rated torque.

Grid line voltage	3.3kV	Rated power	1MW
Load line voltage	3.0kV	Trans,turns ratio(Nn/Np)	1.3
DC bus voltage,Vdc	5600V	Transformer Ls	6%
Transformer Rs	1.2%	No of SM per arm	4
SM cap voltage	1400V	SM capacitance	5mF
Arm inductance,Larm	10%	Switching frequency,fs	1050Hz

Table.1 Parameters of Simulation

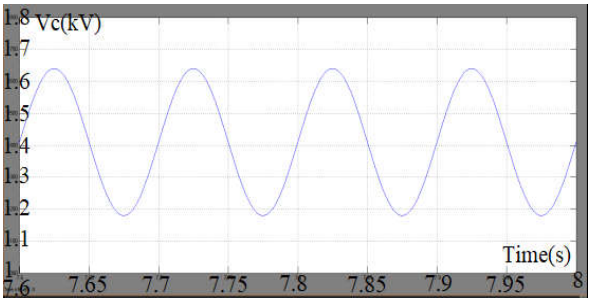


Fig.15: Sub Module(SM) Capacior voltage at output frequency of 0.2 pu and rated torque with Rated dc bus voltage

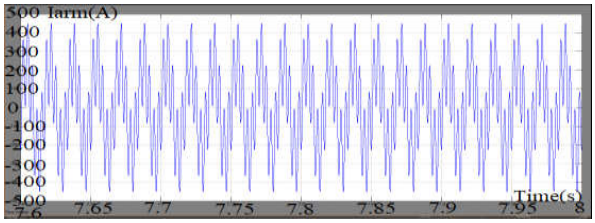


Fig.16 The arm current at output frequency of 0.2 pu and rated torque with hybrid circulating current injection

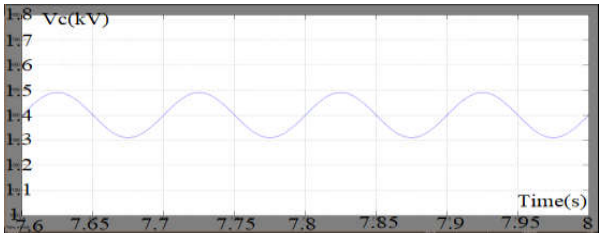


Fig.17: Sub Module(SM) Capacior voltage at output frequency of 0.2 pu and rated torque with 25% rated dc bus voltage

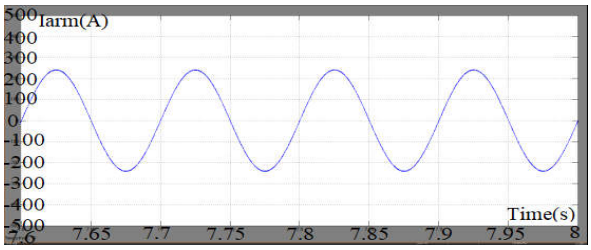


Fig.18: The arm current at output frequency of 0.2 pu and rated torque with 25% of rated dc bus voltage

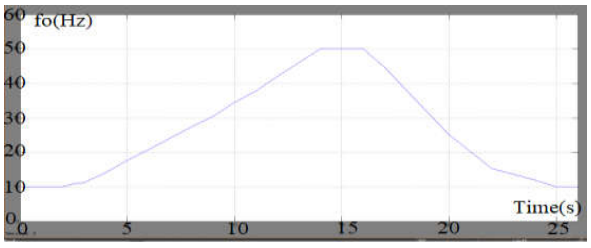
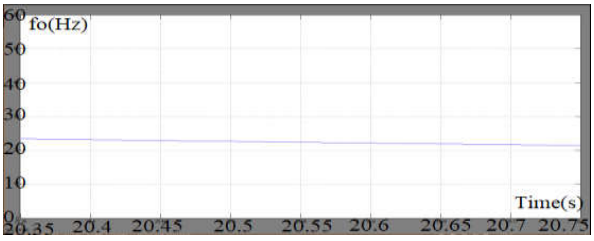


Fig.19: Output Frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s)



FIig.20:Output Frequency when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s) Zoomed at transition of dc bus voltage from 100% to 50% around 20.5se

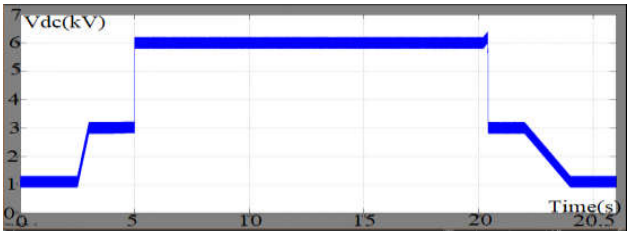


Fig.21:Dc bus voltage when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s)

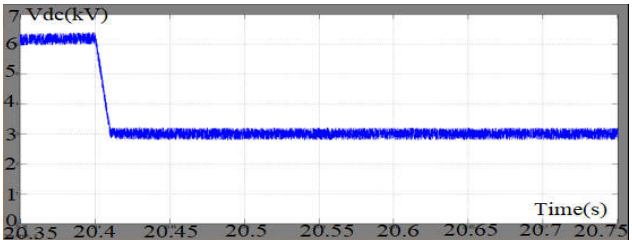


Fig.22: Dc bus voltage when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s) Zoomed at transition of dc bus voltage from 100% to 50% around 20.5se

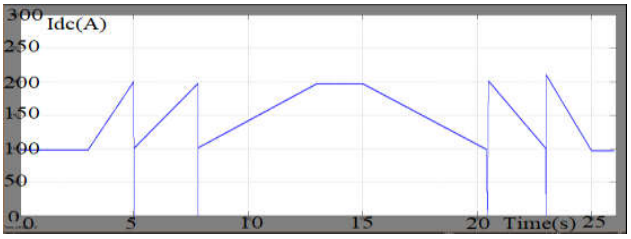


Fig.23: Dc current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s)

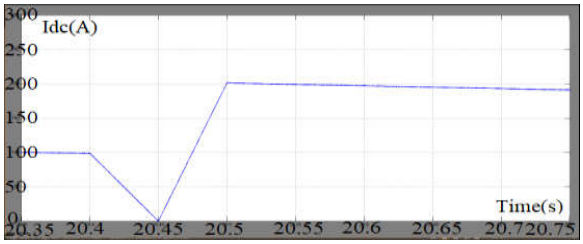


Fig.24 Dc current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s) and Zoomed at transition of dc bus voltage from 100% to 50% around 20.5sec

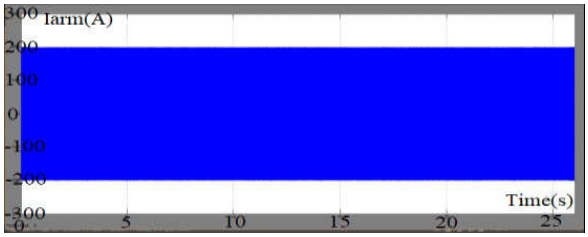


Fig.25 Arm current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s)

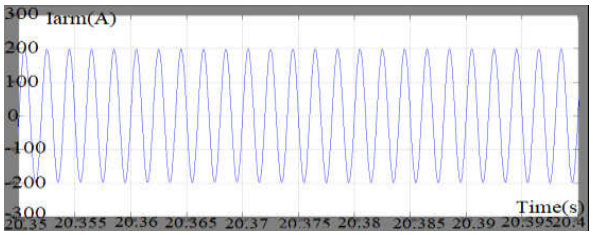


Fig.26:Arm current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s) and Zoomed at transition of dc bus voltage from 100% to 50% around 20.5sec

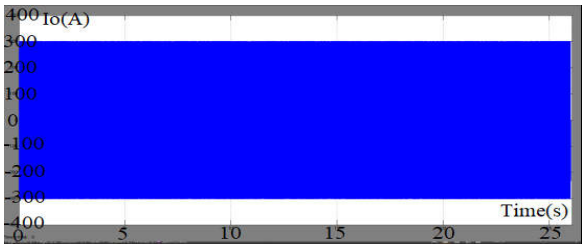


Fig.27:Output current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s)

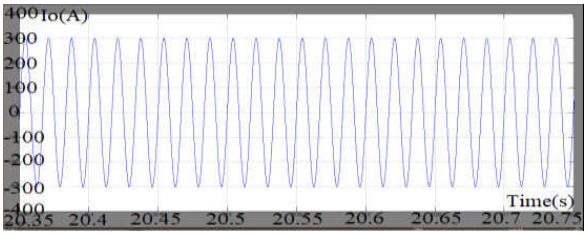


Fig.28:Output current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s) and Zoomed at transition of dc bus voltage from 100% to 50% around 20.5sec

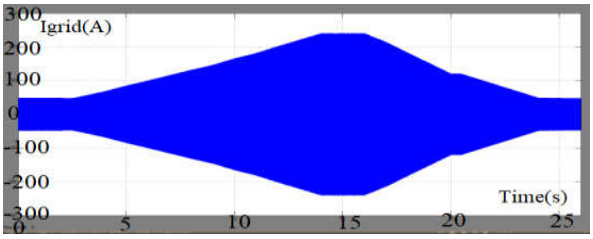


Fig.29:Grid current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s)

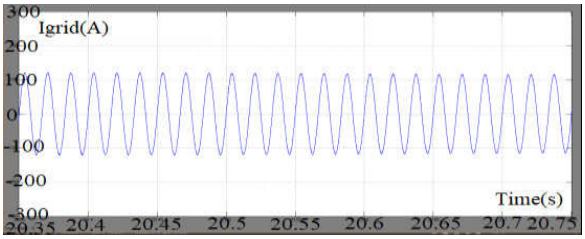


Fig.30:Grid current when the frequency is varied from 4Hz to 50Hz and 50Hz to 4Hz with Time(s) and Zoomed at transition of dc bus voltage from 100% to 50% around 20.5sec

VI. CONCLUSION

The SM capacitor voltage and current ripple are the main drawbacks of MMC based drives when operated at low speed. These ripple can be reduced if the dc bus voltage is reduced at low speed. By using the fuzzy controller in the control technique we can reduce the small variation in the ripples and also the THD value is also reduced than the previous value , a simple method is proposed to reduce the dc bus voltage in MMC based drives, which is fed from multipulse diode bridge rectifiers.When the fuzzy controller is used we can find out the the exact simulation variation than the PI Controller is used,the PI controller is responds only the fixed Kp and Ki values,for the purpose multipulse diode bridge

rectifier is also used to reduce the ripples in the arm current.

The thyristors are switched at zero current only when the dc bus voltage is changed from one level to another level. Another benefit of the proposed configuration is that even if a diode bridge fails, the drive can be operated at reduced power with lower dc bus voltage. This makes the proposed MMC based drive more reliable. Although additional circuitry is required to vary the dc bus voltage, the overall cost of the converter is comparable to that of the existing solutions considering the rating of the components due to additional circulating current. Therefore, it can be an effective solution for high power medium voltage variable speed drives.

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