IMPLEMENTATION OF HIGHER OPERATING TERNARY RIPPLE CARRY ADDER USING CNTFET

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Abstract: Ternary logic is a promising alternative to the conventional binary logic in VLSI design as it provides the advantages of reduced interconnects, higher operating speeds and smaller chip area. This paper presents a pair of circuits for implementing a ternary Ripple carry Adder using carbon nano tube field effect transistors (CNTFETs). The proposed designs combine both futuristic ternary and conventional binary logic design approach. One of the proposed circuits for ternary to binary decoder simplifies further circuit implementation and provides excellent delay and area advantages in data path circuit such as adder. These circuits have been extensively simulated using Xilinx 14.6 to obtain delay and area. The circuit performances are compared with alternative designs reported in recent literature. One of the proposed ternary adders has been demonstrated power, power delay product improvement and with lesser transistor count. So the use of these half adders in complex arithmetic circuits will be advantageous.

I INTRODUCTION

A large part of the success of the MOS transistor is due to its scalability to much smaller dimensions, which results in better performance. This trend still continues in accordance with Moore's law, and silicon-based technology has gone through a phenomenal growth in the last few decades. However, as MOSFETs are approaching their limiting size in the nanometer regime, the semiconductor industry is looking for different materials and alternative devices to integrate with the current silicon-based technology and, in the long run, possibly replace it. Over the past few decades, carbon nanotubes (CNTs) have attracted significant attention in the field of electronics, due to their unique structure and excellent physical properties. Currently, the use of CNTs in the channel region of FET is being investigated experimentally to obtain a new device called carbon nanotube field effect transistor (CNTFET) first demonstrated in 1998. Because of high electron mobility, near ballistic transport, high mechanical and thermal stability of CNTs, CNTFETs are being considered as one of the most promising candidates for post-silicon electronics.

To the best of knowledge of the authors, there is no definitive technique available for the growth of CNTs with required orientation, but the investigations are in progress. A recent paper by George S. et al presented a thorough review on CNTFET. In this, the fabrication of CNT as well as CNTFET, methods to obtain a particular type of CNT purification and proper placement of CNT are discussed. With the current trend of widespread interest in CNTFETs, in near future it may be possible to place required CNTs in the channel region. Though the investigations related to the issues associated with fabrication and purification of CNTs are still continuing, we can explore the possibility of novel circuits using CNTFET for high performance implementation. Nowadays, many studies are going on for designing and exploring the application of CNTFETs in logic gates and benchmarking their performance advantage over the existing MOS technology. The CNTFET circuit application includes binary logic gates ternary logic gate ternary and binary memory cells and multiple-valued logics. The application of CNTFETs for multiple-valued logic has gained keen interest as the threshold voltage of CNTFETs can be controlled by proper selection of the chiral vector of the CNT. Logic circuits as well as different adders, multipliers and memories are also designed to obtain less delay, lower power consumption and to have reduced interconnection complexity. Currently on-chip interconnections have become a serious challenge as more and more modules are packed into a chip. In a typical binary circuit chip 70% of the area is occupied by interconnects, 20% for insulation and only 10% for transistors. These interconnects dissipate lots of energy, increase response time, and cause coupling effects by adding more capacitance, resistance, and inductance to a circuit. Multiple valued logic (MVL) is an alternative solution to interconnect complexity and growing power dissipation by wires. It reduces the amount of wires inside and outside a chip dramatically as more complex designs require a large number of wires for connecting circuit components. Addition is the basic operation involved in most of the arithmetic processing. In the present work two circuits have been proposed for a ternary half adder. Both the circuits exploit the advantages of both multi level ternary and simplified binary circuits. One of the proposed ternary to binary decoder reduces the computational resource required for implementation of ternary adder. This adder circuit gives power and power delay product (PDP) advantages up to 63% and 66% with less transistor count in comparison to a recent reported work. The rest of the paper is organized as follows. A

brief review of multiple-valued logic, CNTFET and its suitability for ternary logic.

II PROPOSED TERNARY ADDER CELL

Ternary logic adds a third value to the conventional binary logic. In this paper, an operating voltage (Vdd) of 0.9 V (as default value of the CNTFET Stanford model of [19]) is used. Therefore, ternary logic values symbolized by '0', '1' and '2' have voltage levels of 0V (ground), 0.45 V (Vdd/2) and 0.9V (Vdd) respectively.

One of the most important and basic ternary arithmetic circuit is a TFA cell. A TFA cell adds three input bits where two bits are ternary 1-bit numbers (A & B) and third bit is Carry signal (Cin) produced from the previous lower significant position (LSB) of n-bit addition, and generates two outputs SUM and Cout. The maximum value of the sum of two 1-bit ternary numbers is 4 at LSB or at most 5 at other positions, which produces Cin at most equal to logic 1. Therefore, Cin will have only two logic values 0 and 1. By utilizing this concept, we designed a TFA cell with ternary nature of A & B and binary nature of Cin in order to get simplicity of the design.

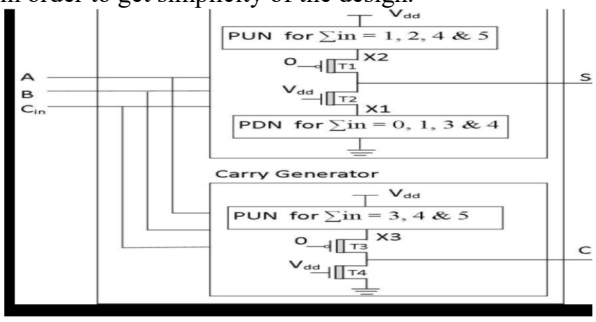

Fig: 1 Schematic diagram of Proposed CNTFET-based TFA cell

The schematic of the proposed CNTFET-based TFA is shown in Fig. 1. The proposed TFA consists of a SUM generator and a Carry generator to produce SUM and Cout signals. The SUM generator contains symmetrical pull-up network (PUN) and pull-down network (PDN) along with resistive voltage divider implemented using two constantly switched ON transistors T1 and T2, to get ternary values of SUM signal. The Carry generator includes only PUN with transistors T3 and T4, due to the binary nature (0, 1) of output carry. Table summarizes how the ON state of corresponding PUN and PDN connect SUM and Cout signals to the appropriate voltage source (Vdd or ground) for each possible summation of input signals (_in). For a SUM generator, when _in = 0, PDN is turned ON which connects SUM to the ground through T2.

Although T1 is also ON, the PUN is OFF. When _in = 1, both PUN and PDN are subsequently ON. T1 and T2 perform voltage division between node voltages X1 and X2, and the result is (X1+X2)/2 which generates logic value 1. When _in = 2, PUN is switched ON and connects SUM to Vdd through T1. As the value of _in increases, SUM signal gets the proper value through PUN, PDN or both. The Carry generator circuit operates in the same way. Transistors T3 and T4 are always switched ON. They perform voltage division between node voltage X3 and ground, and the result is X3/2 whenever Cout has to be 1. When _in becomes more than 2, PUN is switched ON and X3 is 2, then T3 and T4 make Cout equal to 1. Otherwise, Cout is only connected to the ground through T4. From the truth table of TFA and Table I, X1, X2 and X3 signals are derived and can be expressed as

$$X_1 = 0 * \left[A^0\left(B^0\overline{C_{in}}^2 + B^1 C_{in}{}^0 + B^2\overline{C_{in}}^0\right) + A^1\left(B^0 C_{in}{}^0 + B^1\overline{C_{in}}^0 + B^2\overline{C_{in}}^2\right) + A^2\left(B^0\overline{C_{in}}^0 + B^1\overline{C_{in}}^2 + B^2 C_{in}{}^0\right)\right] \quad (1)$$

$$X_2 = 2 * \left[\overline{A^0}\left(\overline{B^0}C_{in}{}^0 + \overline{B^1}C_{in}{}^2 + \overline{B^2} * \overline{C_{in}}^0\right) + \overline{A^1}\left(\overline{B^0}C_{in}{}^2 + \overline{B^1} * \overline{C_{in}}^0 + \overline{B^2}C_{in}{}^0\right) + \overline{A^2}\left(\overline{B^0} * \overline{C_{in}}^0 + \overline{B^1}C_{in}{}^0 + \overline{B^2}C_{in}{}^2\right)\right] \quad (2)$$

$$X_3 = 2 * \left[\overline{A^0} * \overline{B^2} * C_{in}{}^0 + \overline{A^1}\left(\overline{B^2} * \overline{C_{in}}^0 + B^0 C_{in}{}^0\right) + \overline{A^2}\left(B^0\overline{C_{in}}^0 + C_{in}{}^0\right)\right] \quad (3)$$

The schematic of decoder presented in [14] is shown in Fig. 2 (a) where 'B' refers to binary gates. It contains negative ternary inverter (NTI), positive ternary inverter (PTI) and binary gates for the generation of different unary functions.

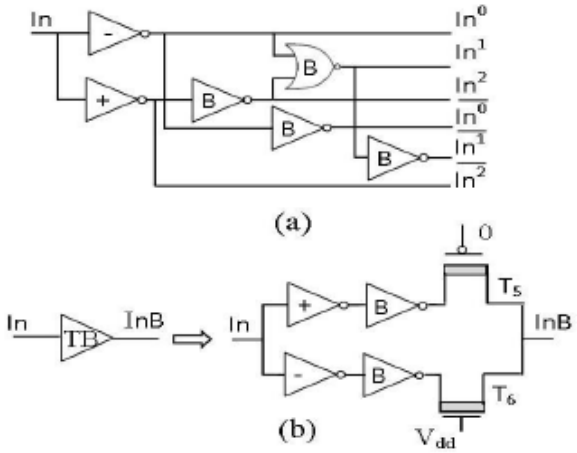

Fig: 2 Schematic diagram of (a) Ternary Decoder (b) Ternary buffer (TB)

The transistor level implementation of the proposed TFA is shown in Fig. 3. PCNTFET (or PU) networks of the SUM and Carry generator are realized based on (2) and (3) respectively, NCNTFET (or PD)

network of the SUM circuit is implemented based on (1). In order to get high performance, these networks utilize transistors with diameter of 1.487nm.

The threshold voltage and chirality vector of these transistors are 0.282V and (19, 0), respectively. Since Ntype and the P-type CNTFETs having same geometry bring about the same resistance and could operate as a voltage divider, two transistors T7 (or T9) and T8 (or T10) with diameter of 1.018 nm are used to generate logic 1 at the output nodes. The threshold voltage of these transistors is taken as 0.413V with the chirality vector of (13, 0). For each possible combination of inputs A, B and Cin, the proposed TFA contains a suitable path that determines the desired output logic. For example, when A = 2, B = 2 and Cin = 0, A2, B2 and Cin0 are 2, and all other true unary functions are 0. Consider SUM generator circuit first N CNTFETs whose gates are connected to A2, B2 and Cin0 switches ON and creates a PD path which makes X1 equal to 0, and PCNTFETs whose gates are connected and Cin2 turn ON and create a PU path to make X2 equal to 2. Then, through voltage division, T7 and T8 produce 1 at the output. Now, in PCNTFET network of Carry generator circuit, transistors whose gates are connected to B0 and _ turn ON and create a PU path to generate X3 equal to 2. Then T9 and T10 perform voltage division and produces 1 at the output. Further, a ternary buffer (referred as 'TB' in Fig. 3) is used at the output to decouple next stage gate inputs with present stage output as well as to provide high performance without sacrificing the overall energy efficiency of the design. The schematic of ternary buffer is shown in Fig. 2 (b). It consists of NTI, PTI, binary inverters and two transistors T5 and T6 with diameter of 1.096nm. The threshold voltage of these transistors is 0.383V with the chirality vector of (14, 0).

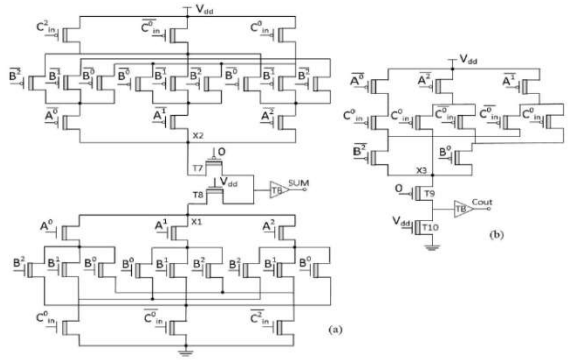

Fig: 3 Transistor level implementation of Proposed CNTFET-based TFA cell

III SIMULATION RESULTS

In this section, the results of simulating two proposed methods are presented. Simulation is done using Xilinx 14.6 simulator. The proposed methods are simulated at different conditions. Figure 3 shows the waveform of output for different combinations of inputs which confirms correct operating of ternary Ripple carry adder. In the following of this paper, we compared proposed method with other existing ternary Half adder designs in different conditions. Average area worth case delay and area-delay product (PDP) are evaluation criteria of the circuits.

The simulation results of RCA is shown in the Fig. 4.

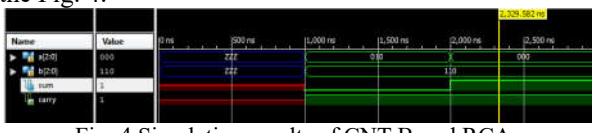

Fig: 4 Simulation results of CNT Based RCA

All input signals have a rise time and a fall time of 6.737ns. A typical rise time delay tr1 is shown in Fig. 5. This is measured when input A is rising from 0 to 1 and the Sum is changing from 0 to 1. Similar procedure is followed to obtain all possible rise time delays and fall time delays for Sum and Carry. The average of all those delays is considered as the delay of the circuit. The average powers consumed by the circuits. Then using these two performance parameters the power delay product is obtained for each design.

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Timing constraint: Default path analysis
  Total number of paths / destination ports: 18 / 2
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Delay:               6.737ns (Levels of Logic = 4)
  Source:            a<0> (PAD)
  Destination:       sum (PAD)

  Data Path: a<0> to sum
                                        Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.222   1.015  a_0_IBUF (a_0_IBUF)
     LUT6:I0->O            1   0.203   0.944  a0/a1/Mxor_sum_xo<0>1 (a0/w<1>)
     LUT6:I0->O            1   0.203   0.579  a0/Mxor_sum_xo<0> (sum_OBUF)
     OBUF:I->O                 2.571          sum_OBUF (sum)
    ----------------------------------------
    Total                      6.737ns (4.199ns logic, 2.538ns route)
                                       (62.3% logic, 37.7% route)
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Fig: 5 Timing Report of Proposed method

The analysis of the table indicates that for the proposed designs, the circuit complexity is less than the previous reported design [5]. The transistor count of Design1 is reduced from 130 to 94. This design also consumes 12% less power with less delay. The PDP is reduced by 15%. The Design2 with new decoder uses only 66 transistors. The reduction in delay, power and PDP for this design are 9% , 63% and 66% respectively, compared to the earlier reported design [5].

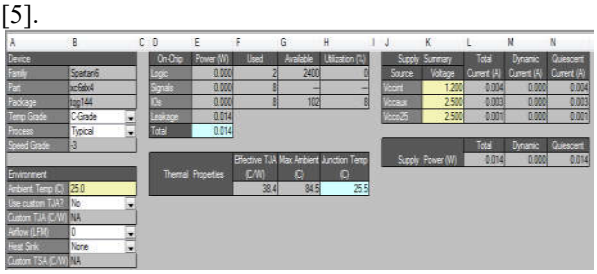

Fig: 6 Power Consumption of Proposed Method

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	200	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	200	0%	
Number of OLOGIC2/OSERDES2s	0	200	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	8	0%	
Number of ICAPs	0	1	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	1.75			

Fig: 7 Device Utilization Summery of Proposed Method

CONCLUSION

This paper has proposed a novel design of ternary Ripple carry adder cell (TFA) using CNTFETs. The proposed TFA uses a resistive voltage divider as an integral part of the design and output buffer. The given structure outshines the existing TFA circuits in terms of delay and energy consumption. In addition, it has high driving power and is robust. Further, a three-input ternary XOR circuit is also formed by using the concept of modulo-3 addition. This design also benefits from high energy efficiency. Based on simulations with XILINX 14.6, using the CNTFET compact model of Stand ford, the circuit performances are compared with the best reported half adder circuit. Simulation results have confirmed that the proposed logic circuits achieve power and delay improvements than the alternative design. One of our proposed novel design gives reduction in delay, area and PDP by 9%, 63% respectively compared to the earlier reported design. This approach of adder design can be used for complex arithmetic circuits using futuristic CNTFET devices.

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