Implementation of Reversible Wallace Multiplier using Multiplexed Based Full Adder

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Abstract

Reversible logic circuits are inexorable in quantum computers in which designing area efficient architectures play key role, which decides the cost of the chip. Area efficiency can be achieved by using proper logic optimization technique in reversible logic circuits. In this paper, Reversible Wallace multiplier is designed by using multiplexed based full adder. Implementation of proposed architecture and conventional reversible architecture is carried out on Vivado v2017.2 software. The performance evaluation results show that the modified architecture is area efficient in terms of LUT's

Keywords: Adders, Logic optimization, LUTS, Reversible logic, Wallace multiplier.

I. INTRODUCTION

Reversible logic circuits are contemplated as feasible means for achieving power efficiency in quantum computer, optical data processing, Nano technology. Reversible logic means its input and output be uniquely retrievable from each other and they have one –to- one mapping between vectors of inputs and outputs[1].

Even though the structure of reversible logic is difficult when compared to irreversible logic circuits, there is a need to reduce power as well as area to decrease the chip cost. The performance evaluation for such a circuitry can be decided by the elements such as gate count, delay ,garbage outputs , constant inputs , quantum cost and the complexity of the hardware. Hence, in order to improve the performance of reversible circuits, there is a need to improve the performance of the above said elements. In present day scenario, there are several multipliers, which are compatible to the reversible logic.From literature Survey, it has been observed that array multiplier, serial multiplier consumes more area, power and also speed is very less. Whereas Wallace multiplier gained importance in performing fast computations[2]-[3]. It has also been studied from literature survey that multiplexer based adders gain importance because of the chip area reduction.

The rest of the paper is structured as follows. Section 2 describes about Preliminaries. Section 3 deals with Reversible Wallace multiplier using modified

reversible multiplexer based full adder.Section 4 deals with the synthesis, simulation results and comparison Finally, Section 5 concludes the work done.

2. Preliminaries

The main gates used for developing reversible architecture are discussed in this section.They are Feynman gate, Toffoli gate, Peres Gate, Fredkin gate, New gate Syman Gate.

2.1 Feyman gate

Feyman gate is also known as Controlled-NOT gate(CNOT) .It is a 2×2 reversible logic gate.[1].The equations for realizing Feyman gate are shown in Eq.(1) & Eq.(2).

$$P = A \quad (1)$$

$$Q = A\hat{}B \quad (2)$$

Where '^' indicates XOR operation

2.2 Toffoli gate

Toffoli gate is also known as Controlled-Controlled NOT gate(CCNOT).It is a 3×3 reversible logic. When the third input is logic **0,** the output is **AND** of given two inputs.The equations for realizing Toffoli gate are shown in Eq.(3),Eq.(4) & Eq.(5).

$$P = A \quad (3)$$

$$Q = B \quad (4)$$

$$R = A\,B\hat{}C \quad (5)$$

2.3 Peres gate

The schematic diagram for Reversible Peres gate is shown in Fig.1.Constant inputs are input lines which are always either **0** or **1.**the outputs which are not used are called garbage values. The cost of circuit in terms of cost of primitive gates (1×1 or 2×2)arereferred to as quantum cost. The schematic diagram for quantum realization is shown in Fig.2.Hardware complexity is defined as total number of logic operations in the reversible circuit. The main terms in hardware complexity are α(2 input XOR gates),β(2 input AND gate),δ(NOT gate).Therefore hardware complexity = a.α + b.β + c.δ, where a,b,c are number of operations in output expression. For peres gate input vector (I_v)=(A,B,C)and output vector (O_v)=(P,Q,R).Therefore quantum cost and hardware complexity are **4** and **2**α **+1**β.

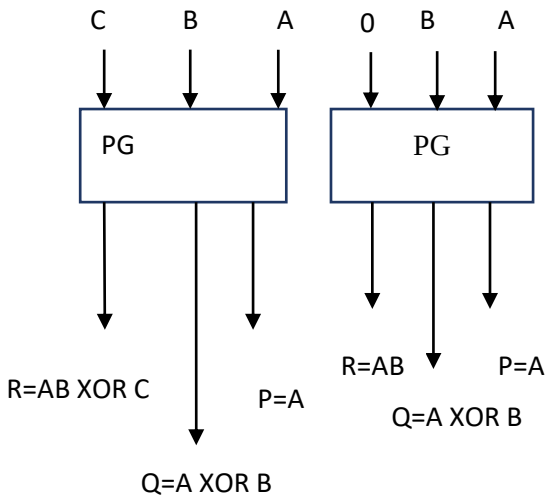

Figure 1.Schematic diagram for Reversible Peres Gate

A,B,C are given as inputs to Reversible Peres gate and P,Q and R as taken as outputs.The functionality can be observed by using the table.I and Eq.(6),Eq.(7) and Eq.(8)

$$P = A \quad (6)$$
$$Q = A\hat{}B \quad (7)$$
$$R = AB\hat{}C \quad (8)$$

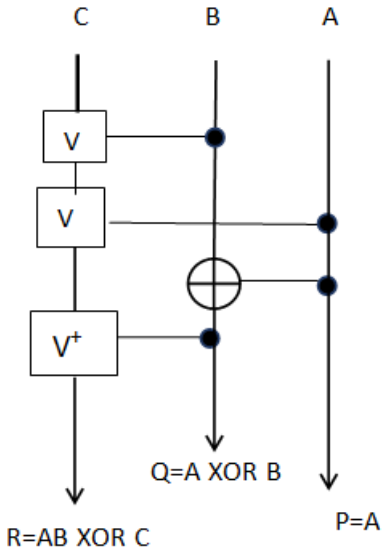

Figure 2.Schematic diagram for Quantum Realizationfor Reversible Peres Gate

Table .1. Truth table of Reversible Peres Gate

INPUT			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

2.4.Reversible Full Adder

It is a 4×4 logic reversible logic. The first two outputs are considered as garbage values which are not used in present adder. Generally the fourth input is given as logic **0.**Here the inputs are considered as A,B,C and the outputs as R,S .The schematic diagram and Quantum realization are shown in Fig.3 & Fig.4 respectively.

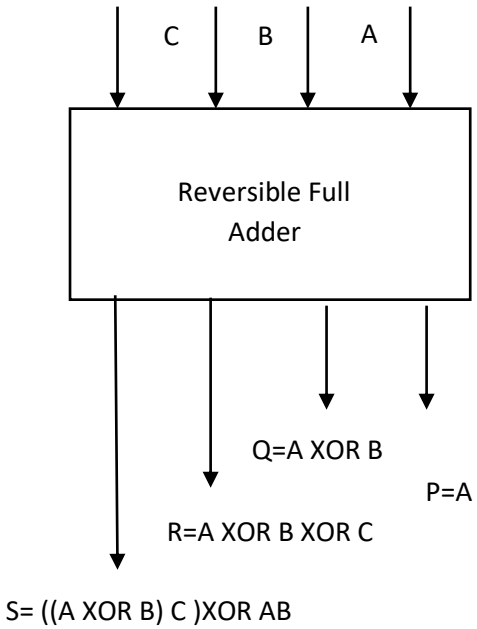

Fig.3.Schematic diagram for Reversible Full Adder

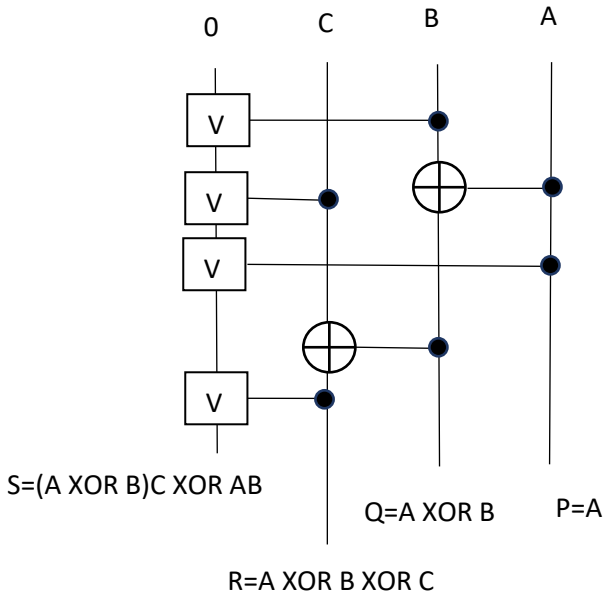

Figure 4.Schematic diagram for Quantum Realization forReversible Full Adder

3.Reversible Wallace Multiplier using Reversible Multiplexed Based Full Adder

In this section a 4×4 Reversible Wallacemultiplier of inputs X (X_3… X_1X_0) and Y(Y_3…Y_1Y_0) and output Z(Z_7…Z_1Z_0)is discussed. The 16 partial products (X_3Y_3,X_2Y_3,..X_1Y_0,X_0Y_0) are calculated initially. The 3 partial products of same values are fed to reversible full adders, and 2 partial products are fed to peres gates. If any partial products are left they are fed to second stage adders. In second stage left over partial products and sum, carry of first stage are used as inputs.In third stage ripple carry adders are used to produce outputZ.The schematic diagram for modified Reversible Wallace multiplier is shown in Fig.5.

3.1Reversible Multiplexed Based Full Adder(RMBA)

Reversible Multiplexed based Full Adder(RMBA) decreases the time delay and power consumption which are basic parameters in VLSI circuits. It is a 4×4 logic reversible logic .The first two outputs are considered as garbage values which are not used in present adder. Generally the fourth input is given as logic **0.**Here the inputs are considered as A,B,C and the outputs are taken as V,W,S,C. The schematic diagram for modified Reversible Multiplexed based Full Adder(RMBA) is shown in Fig.6.

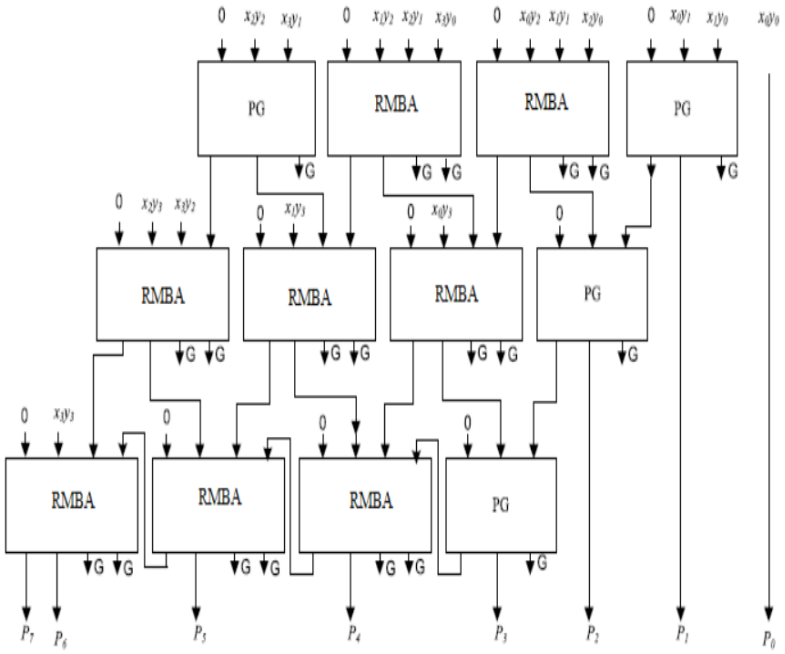

Figure 5.Reversible Wallace Multiplier using Reversible Multiplexed Based Full Adder.

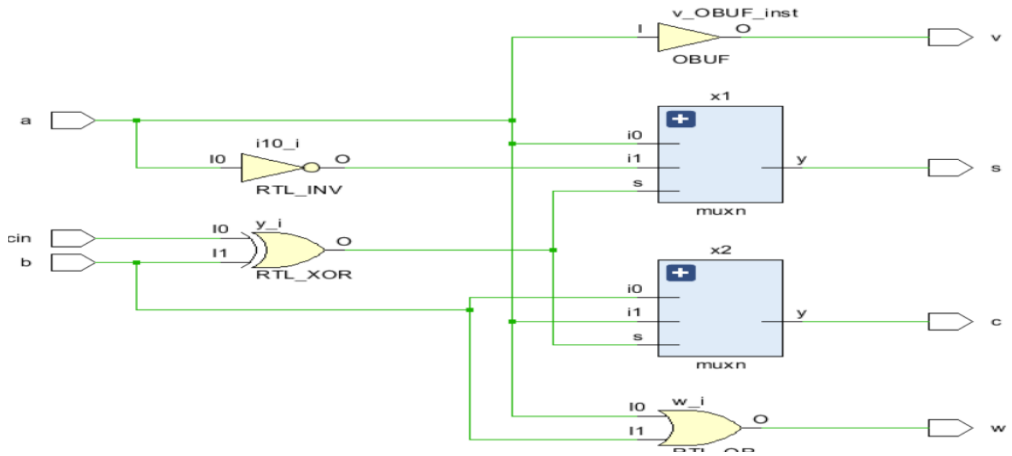

Figure 6. Schematic diagram for Reversible Multiplexed based Full Adder(RMBA)

4. Results and Comparisons

Reversible Wallace architecture consists of peres gates and reversible full adders. The conventional and modified reversible Wallace multipliers for 8-bit have been stimulated with different reversible adder logics and the performance analysis is tabulated in Table.2From Table.2, it is observed that area is reduced by 25%,23.17% and 12.19% for RMBA(FA2) when compared to Reversible Wallace, Wallace andReversible Wallace using modifies Full Adder(FN) respectively.Bar diagram shown in Fig.7 represents LUT delay product for different multipliers.Bar diagram represents shown in Fig.8 represents power delay product for different multipliers

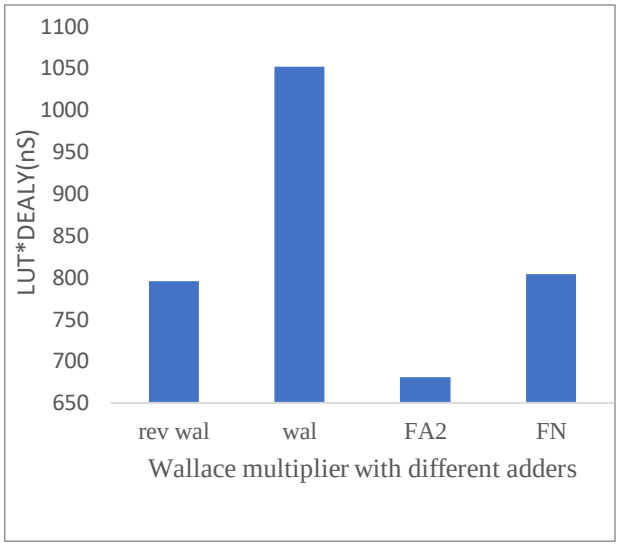

Figure 7.Comparison of LUT- Delay Product for different multipliers

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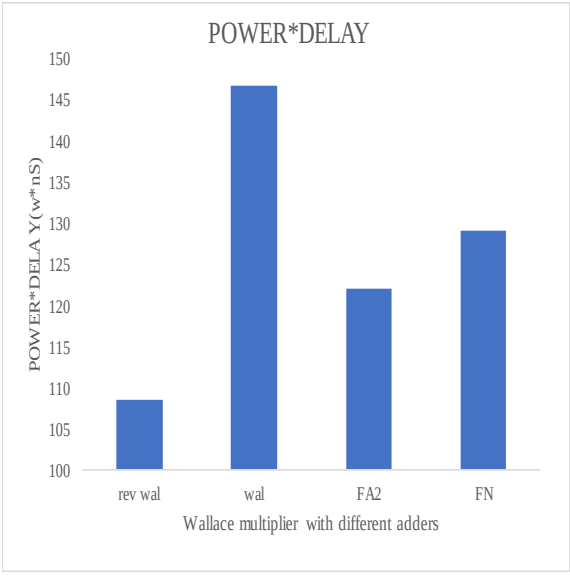

Figure 8.Comparison of Power -Delay Product for different multipliers

.**Table 2. Performance Analysis for different multipliers**

Multiplier	LUT	Power (W)	Delay (ns)
Reversible Wallace	103	14.05	7.721
Wallace	101	14.089	10.411
Reversible Wallace using modified Full Adder(FN)[5]	92	14.78	8.734
Reversible Wallace using multiplexed based Full Adder (FA2)	82	14.691	8.299

5. Conclusion

Design of Reversible Wallace multiplier using Multiplexer based full adder is carried out in this paper. From the results, it has been concluded that the modified architecture shows better improvement in area when compared to different multiplier configurations. Thus the proposed design is said to be an area efficient architecture .

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