Design of 18-Transistor TSPC Flip-Flop Based on Logic Structure Reduction Schemes

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Abstract

High performance VLSI chip design, latches and flip-flops have a direct impact on power consumption and speed of VLSI system. As these flip-flop topologies have low power consumption and small area can be used in various applications like digital VLSI clocking system, buffers registers, microprocessors. A most high performance flip-flop is the True single-phase clocking flip-flop design. A low-power true single-phase clocking Flip-Flop (FF) design follows a master slave logic structure with features like a hybrid logic design comprising both static CMOS logic and complementary pass transistor logic. The logic structure reduction scheme is employed to reduce the number of transistors for achieving high power and delay performance with an objective of lowering the clock signal loading.

In the design implementation, transistors sizes are optimized with respect to the Power Delay Product (PDP). The performance levels of five FF designs (21 transistor), (22 transistor), (19 transistor), (18 transistor), the timing parameters of each FF designs were compared using 130-nm CMOS Process Technology in Mentor Graphics tool. The simulation results shows that the proposed design excelled in various performances indices such as PDP, power consumption, clock to Q delay, data to Q delay. Compared with the conventional TGFF designs, simulation on process corners, supply voltage settings, and working frequencies were conducted to study the design reliability.

Keywords: *Complementary Pass-Transistor Logic (CPTL), Flip-Flop (FF), True Single Phase Clocking (TSPC)*

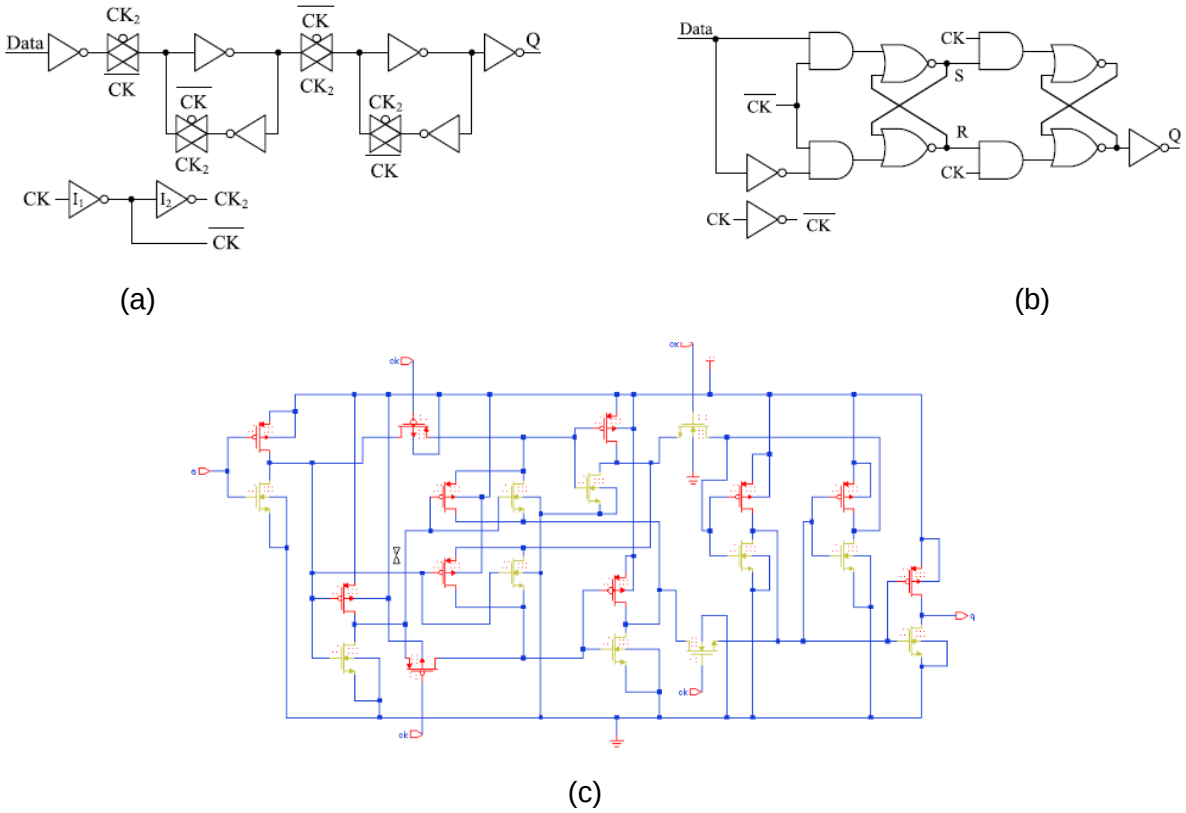
Introduction

Flip-flops are basic building blocks in the memory of electronic devices. Each Flip-Flop stores one bit of data. Flip-flop modules such as registers files, shift registers, and FIFO[1]. The Flip-Flops uses both static and dynamic logic. It consists of various types, in this paper master slave flip flop is employed to achieve low power design. The Flip-Flops are mainly used as a memory storing elements in mobile phones, digital camera and tablet PC [3].

FF designs undergo continuous improvement with the advances in new process technology. Specific application demands such as high speed, low power, and low voltage also call for new FF designs. In this paper, a low-power FF design meeting these requirements is investigated. A true single clocking Flip-Flop design has been developed with the objective of lowering clock signal loading. A transmission gate based FF is designed, one possible drawback of the design is the excessive work load on the clock signal where complementary signals are required, to avoid this, a cross coupled set-reset latches are used in lieu of the transmission based latch to support single clock–phase operation[1].

The design follows the theory of TSPC execution to allay the clock signal loading. The logic structure reduction and transistor optimization schemes are applied to optimize the design [1].

The operation of the Master-Slave flip-flop is that clock pulse is 0, the PMOS transistor connected to CP turns on and the master latch becomes the data input mode. Both the voltages VD1 and VD2 are pulled up to power-supply level and the data from D are stored in the master latch. When the clock pulse is 1, the PMOS connected to CP turns off, the NMOS connected to the CP turns on, and the slave latch becomes the data output mode. Then the data stored in the master latch is transferred to the slave latch and then outputted to Q. In this operation, the master and slave latch become active alternatively so there is small time degradation on cell performance [2].



(a) (b)

(c)

Fig. 1. Conventional fully static FF designs (a) TGFF (b) SRFF (c) ACFF

Review of Existing FF Design

To provide a basis for comparison, some existing FF designs are reviewed first. A classic master–slave-type TGFF design is shown in Fig.1(a), indicating that it comprises two TG-based latch designs. Inverters *I*1 and *I*2 are used to generate complementary clock signals. This design suffers from a high capacitive clock loading problem (a total of 12 transistors driven by the clock), which indicates a sustained power consumption even when the input remains static. This problem also occurs in conventional SRFF designs, as shown in Fig.1(b). To overcome the power consumption problem, two FF designs employing an adaptive coupling (AC) technique and a topologically compressed scheme have been proposed. Fig.1(c) shows the AC FF design, unlike conventional TGFF designs, this design uses a differential latch structure with pass-transistor logic to achieve TSPC operation.

The TGs are replaced with either n- or p-type pass transistors. To overcome the impact of process variations on the master latch, a pair of level restoring circuits is inserted into the cross-coupled paths of the master latch. In this design, only four MOS transistors (two PMOS and two NMOS) are driven by the clock signal, and the transistor count is lowered to 22. A lighter clock loading in addition to the circuit simplification of the FF design can lower the power consumption significantly. In this design, the data contention problem in the slave latch deteriorates as the data switching activity increases, and the advantages of power saving are thus diminished. The level restoring circuit pair of the master latch results in a longer setup time. Moreover, this design suffers from a power leaking problem when certain input and internal node combinations occur [1].

The SR- latch based TSPC FF design named topologically compressed FF (TCFF), obtained through a topologically compressed schemes, the logic schematic of this design is shown in Fig. 2(a), and the MOS circuit is shown in Fig.2(b). The TCFF design based on the single clock pulse, reduce the number the transistor driven clock, and reduce the total transistor count. The master latch adopts the configuration of a MUX with feedback and can be implemented with two AND-OR-Invert (AOI) gates and an inverter. When CK is 0 then the latch is transparent, then the input pass through AOI gates and the node X3 i.e. the output is complementary to the input. When CK is 1, the input data is blocked and the output node of X3 remains unchanged because of the closed path. The slave latch also comprises of two AOI gates and an inverter, but only one phase of the clock signal is used. The MOS circuit in Fig. 2(b) is optimized, for N(pull down) logic, one CK-controlled NMOS transistor can be shared by the two discharging paths. For P(pull up) logic, four pairs of PMOS transistors are connected to VDD, and two of these pairs share identical inputs, two pairs of the master latch can be eliminated. The node *x*2- or *x*3-controlled PMOS transistors will turn ON through the addition of an extra clock controlled PMOS transistor across the two AOI gates can be removed without affecting the function, the circuit is shown in Fig.2(c). reducing count from 22 to 21.

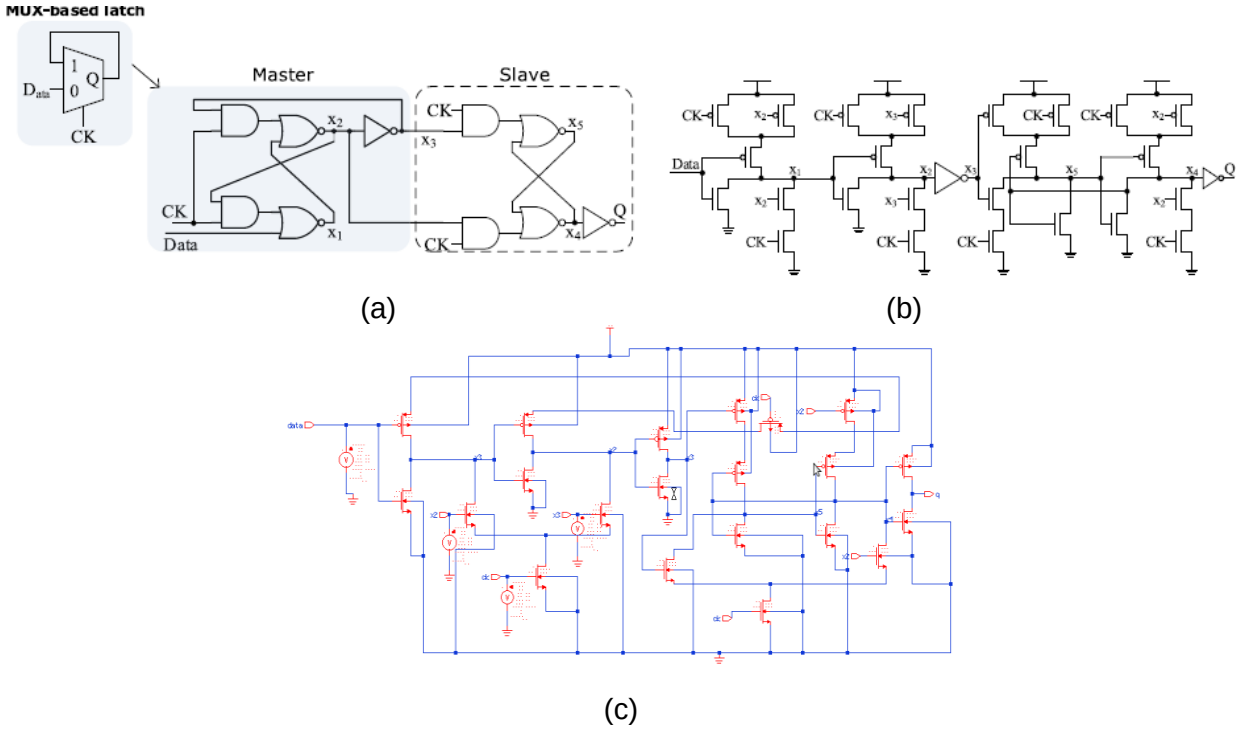


Fig. 2. TCFF. (a) logic structure. (b) MOS circuit schematic(28 transistor). (c) TCFF(21tranistor)

This design is fully static, even though both pull-up and pull-down logic networks are largely simplified, hence the conclusion of TCFF based on 3 principles: 1) reduces the number of transistors, 2)reduces the transistor count, 3)use only single clock phased clock, the design suffers from longer step-up time. So, to reduce the time delay LRFF is used to reduce the power consumption Fig.3 shows the diagram of LRFF, named logic structure reduction schemes, is the enhancement of TCFF in different performance aspects, In this aspect the three measures taken under consideration: the measures are the shorter set-up time, the power leakage problems and the elimination of the node floating cases. Here the discharging path is split into two path comprising of two NMOS transistors in series implementing x2.CK.0 and x3.CK.0. Hence the transistor count is reduced to 21 to 19.

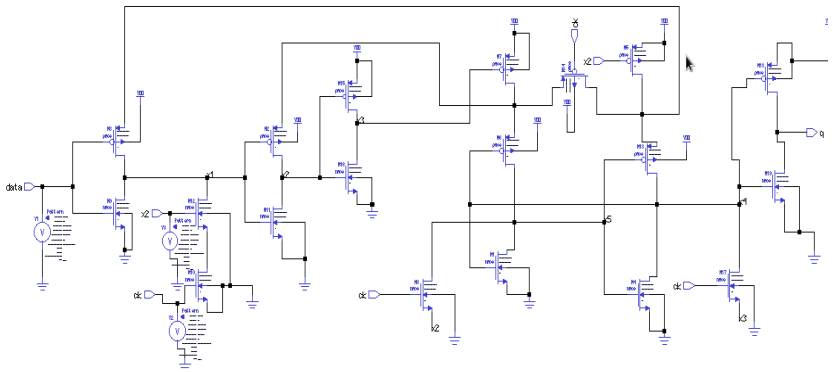


Fig. 3. LRFF(Logic Structutre Reduction Schemes Flip-flop)

The total number of transistors is only 19. Only one single phase of the clock is required, and the fan-out for the clock signal is four (one PMOS and three NMOS transistors).The proposed LRFF is fully static and can avoid the case of temporary output node floating. When CPL is introduced, the circuit complexity of its p-logic network is largely reduced, even though the design is not a dynamic logic, hence the transistor count is reduced to 19 to18 transistor Flip-Flop. In the proposed system design the transistor count is further reduced from 19 to 18.

Proposed Design

This reduction simplifies the circuit and the power consumption is also reduced. Fig.4 shows the structure of 18 transistor FF design. In this design the transistor in the master latch is combined with the clock signaland changes its value i.e, the data stored in the master is transferred to slave and its output to Q and thus the transistor count is reduced by one.

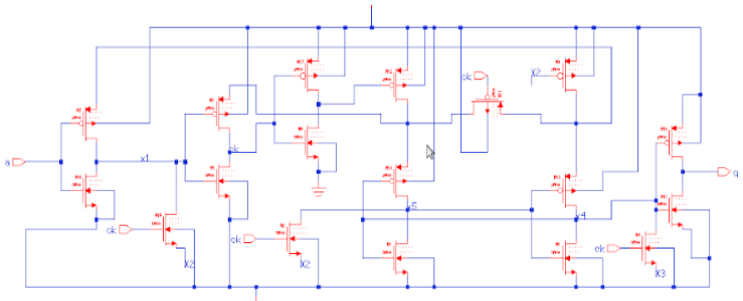


Fig. 4. Proposed circuit 18 transistor TSPC Flip-Flop design

Change its value that is the data stored in the master is transferred to slave and it is outputted to Q and thus the transistor count is reduced by one. The clock controlled NMOS transistor is also connected with the x2 discharging node. Hence, the power gets reduced and the delay also compromised.Fig.5 shows the simulation results and Fig.8 shows the layout diagrams for Flip-flop designs

Simulation Results

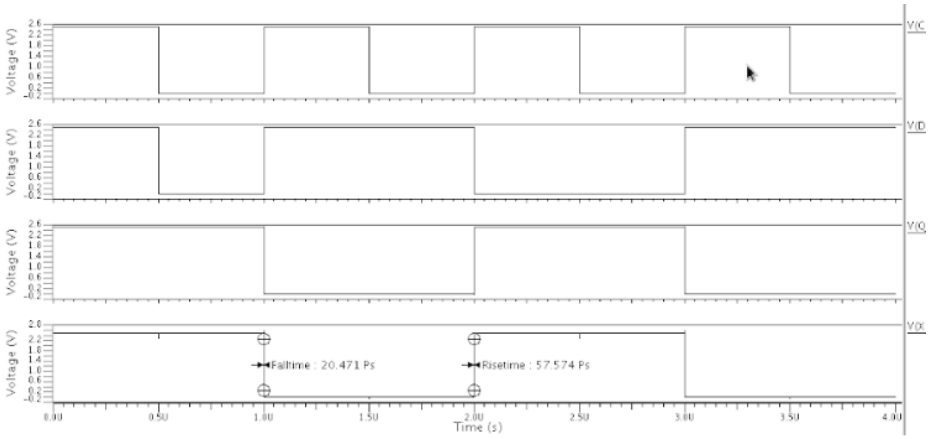
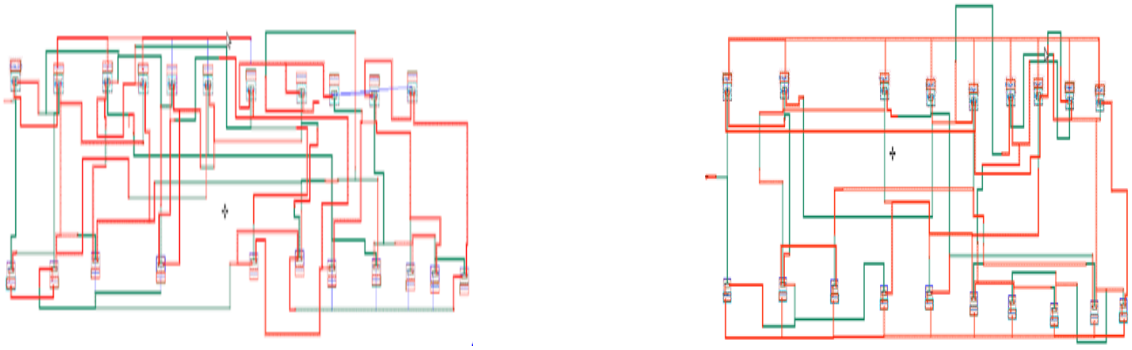


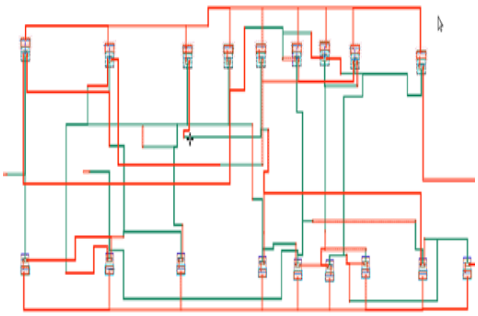
Fig.5. Simulation results for 18 Transistor Flip-Flop

Table 1 shows the comparison of power dissipations between the base paper [1] and the implemented work.

FF DESIGNS	TGFF	TCFF	LRFF	PLRFF
NO OF TRANSISTORS	22	21	19	18
AVERAGE POWER (nw)	22.641	21.221	14.9194	9.632
CLK TO Q DELAY (ns)	36.822	35.128	33.976	31.423
DATA-TO-Q DELAY(ns)	10.037	10.001	9.976	9.874
PDP_{CQ}	0.833	0.791	0.596	0.370
PDP_{DQ}	0.227	0.225	0.148	0.098



(a) (b)



(c)

Fig.6. Layout schematic of the FF designs. (a) TGFF (b) LRFF (C) PLRFF (18 trans.)

Power performances under VDD=1V conditions

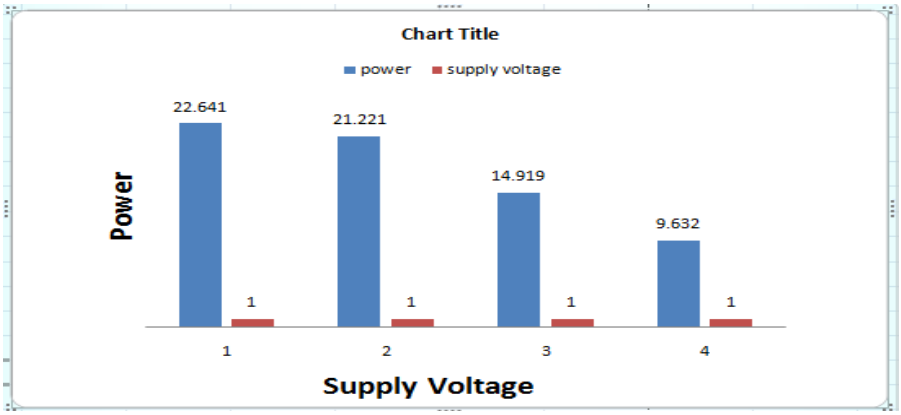


Fig.7. power performance under VDD=1V

Fig.7. represents the power evaluation conducted under VDD settings varying from a nominal 1V. the power advantage of the proposed design was consistent under all VDD settings. Compare to TGFF design, the power saving of the proposed is varied from 40.3% (VDD=1).

Conclusion

The Flip-flop design achieved by employing a modified SR latch structure incorporating a hybrid logic consisting of static-CMOS logic and CPL. The proposed method was determined to excel in power performance and consistently outperformed other methods under different voltage and switching activity settings using CMOS130 nm technology in Mentor Graphics tool It can eliminate the clock skews caused by different clock phases are generated off-chip which significantly saves chip area and power consumption. In particular, the proposed design consistently outperformed other design under different voltage and switching activity settings. Thus proves the efficiency of the proposed FF design

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