DESIGN OF LOW AREA BIST FOR SCAN-BASED LOGIC CIRCUITS

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ABSTRACT: In an arbitrary testing condition, a lot of amount is wasted in the LFSR and in the CUT by examples that don't add to fault dropping. Another real wellspring of vitality waste is the misfortune because of irregular exchanging movement in the CUT and in the sweep way between utilization of two progressive vectors. In this work, another built-in self-test (BIST) conspire for sweep based circuits is proposed for lessening such region utilization. A mapping rationale is structured which alters the state advances of the LFSR to such an extent that just the valuable vectors are produced by a desired sequence. Experimental results on benchmark circuits uncover a lot of region reserve funds in the LFSR irregular testing.

KEY WORDS: BIST, power droop (PD), test pattern generator (TPG), Linear Feedback Shift Register (LFSR), Multiple Input Signature Register (MISR)], pseudorandom test generator (PRTG).

I.INTRODUCTION

Scan-based BIST integrates scan design and built-in self-test methodologies. Using scan, the memory elements are connected into a shift register and thus their values can be controlled or observed during the test mode by shifting the desired values into the register or shifting out the content of the register. BIST is a technique that makes the circuit test itself without using automatic test equipment. It includes on-chip test pattem generator (TPG) [for e.g., Linear Feedback Shift Register (LFSR)] and response analyzer [for e.g., Multiple Input Signature Register (MISR)].The LFSR is commonly used as a TPG in low overhead BIST schemes. The correlation between consecutive random patterns generated by an LFSR is low but a significant correlation exists between Consecutive patterns at the primary inputs (PIs) during the normal operation of circuit.

For DFT, the situation is even worse. Here, during test mode, it breaks all the secondary input (SI) and secondary output (SO) to apply any desired value at state FFs i.e. breaks a sequential circuit into a combinational block and state elements (scan elements/D FFs). This destroys the correlation that typically exists between successive states of FSM leading to even lesser correlation.

The forceful scaling of microelectronic innovation is empowering the manufacture of progressively complex ICs. Together with a few advantages (enhanced execution, diminished expense per work, and so forth.), this stances genuine difficulties as far as test and dependability. Specifically, amid at-speed trial of superior chip, the IC activity factor (AF) incited by the connected test vectors is altogether higher than that accomplished amid in field task. Thusly, excessive power droop (PD) might be produced, which will back off the circuit under test (CUT) flag changes.

Thus, a false test come up short will be produced, with ensuing increment in yield misfortune. At-speed trial of rationale squares is these days oftentimes performed utilizing Logic BIST which can appear as either combinational LBIST or sweep based BIST, contingent upon whether the CUT is a combinational circuit or a consecutive one with output. In case of scan-based BIST, two basic capture-clocking schemes exist:
1) The launch-on-shift (LOS) scheme and
2) The launch-on-capture (LOC) scheme.

In LOS plans, test vectors are connected to the CUT at the last clock (CK) of the move

stage, and the CUT reaction is examined on the sweep chains at the accompanying catch CK. In the LOC plot, rather, test vectors are first stacked into the output chains amid the move stage; at that point, in a following catch stage, they are first connected to the CUT at a dispatch CK, and the CUT reaction is caught on the sweep chains in a following catch CK. Test length of sweep based BIST is normally controlled by the difficult to-test issues. Test length decrease of the difficult to-test deficiencies is an essential issue. Various techniques are used to handling the problem.

1) A combination of the deterministic test patterns of the hard-to-test faults with random patterns, where all deterministic tests are stored in the system before testing. Test data compression is an important issue for these techniques.
2) Weighted test pattern generation that applies weighted tests to the primary inputs. However, only application of weighted patterns to primary inputs may not solve the problem completely.
3) Test point insertion that can make a lot of random resistant faults testable

They experience the ill effects of the PD issues examined above, particularly amid the catch stage, because of the high AF of the CUT instigated by the connected test designs. Arrangements enabling originators to lessen PD amid the catch stage in output based BIST are in this way required. While a few methodologies have been proposed to decrease PD for combinational BIST, just a couple of arrangements exist for sweep based BIST.In, a test design generator with a preselected flipping level is introduced. It empowers over half decrease in the AF of the output chains by preselecting the quantity of move cycles amid which the sweep chains are stacked with steady rationale esteems. In any case, it requires over 60% expansion in the quantity of test vectors (consequently TT) to accomplish indistinguishable FC from with ordinary output based BIST. The arrangement depends on embedding's an extra stage, in particular a burst stage, between each move and catch stage. Such a burst stage goes for expanding the current drawn from the power supply, up to an esteem like that consumed by the CUT amid catch stages. Along these lines, the inductive part of PD happens amid the burst stage, and vanishes before the accompanying catch stage. This arrangement causes an expansion in both the aggregate power devoured amid test and TT

II. PRELIMINARIES

First, we present several necessary definitions. An output cycle is the period in which a test design is moved into (or test reactions are moved out of) the sweep chains. The length of a sweep cycle (the quantity of clock cycles) is equivalent to the quantity of output flip-slumps in the longest output chain. A catch cycle is the period between two nearby sweep cycles. The circuit is set to the ordinary mode amid the period when the test design is connected to the circuit and the test reactions are caught in the sweep flip-flops. Usually, a capture cycle is a single clock cycle; however, the test schemes proposed apply multiple capture cycles. That is, the circuit is set to the typical mode for numerous clock cycles after the move cycles. A test cycle comprises of an output cycle pursued by a catch cycle. The - controllability of a hub is characterized as the likelihood of supporting at hub by an arbitrarily chosen information vector. The recognisability is characterized as the likelihood of engendering the estimation of by an arbitrarily chosen info vector to an essential yield. The detection probability of fault is characterized as the probability to distinguish the blame (stuck-at) by an arbitrarily chosen information vector.

The detectability is defined as the probability for the fault to be detected by the first randomly selected input vectors. A number of the previous scan-based

methods used the stumps scan-based BIST architecture. The outputs of the pseudorandom test generator (PRTG) are connected with a PS. Each of the extra pins of control test points is directly connected with one bit of the outputs of the PS. Therefore, the number of control test points cannot be large enough. This may make the method unable to get good enough testability in many cases. Each scan chain is also connected with one bit of the PS. Each output of the scan chains is connected with one bit of the MISR. The observation test points are also connected with inputs of the MISR. A new scan-based architecture is presented, where the control points are connected with the outputs of the PRTG or PPIs. Connection of a control point with an output of the PRTG or a PPI generates no new convergent fan outs in the combinational part of the circuit. Furthermore, more than one control test points can be connected with the same output of the PRTG. Similarly, the extra inputs of control points can also be connected with any PPIs, that is, outputs of scan flip-flops. Each scan chain is partitioned into multiple scan segments, and an XOR gate is inserted between two adjacent scan segments. Outputs of all scan segments are connected to an exclusive-or tree. Our method does not insert any other extra observation points to improve testability. However, the extra connections from the outputs of the scan segments with the XOR gates are similar to extra observation points, which can effectively improve observability of the circuit. A capture cycle follows a number of shift cycles, whose number is equal to the number of scan flip-flops in the longest scan segment. The proposed scan-based BIST architecture can capture test responses much more frequently, and therefore, can substantially reduce test-application cost.

III. RELATED WORK

BIST schemes can be classified into (a) test-per-clock and (b) test-per-scan. In test-per-clock BIST (Fig. 1), the outputs of a test pattern generator are directly connected to the inputs of a CUT and a new test pattern is applied to the inputs of the CUT at every clock. Also, the response to a test pattern applied to the CUT is loaded into a response analyser at every test cycle. BILBO and circular BIST are the examples of test-per-clock BIST. A scan chain partitioning scheme is introduced in BIST to optimize the number and the length of scan chains. Each of the scan chains is partitioned into multiple segments, where an XOR gate is inserted between two adjacent segments. One input of the XOR gate is connected with the scan-in signal of the scan chain, and the other is connected with the output of the preceding segment. Let the length of a scan segment be. The input signal of each scan segment except the first one is the exclusive-or of the value of the scan-in signal and the value of the output of the previous scan segment. Outputs of all scan segments are connected with an XOR tree, whose output is connected with one stage of the MISR.

The test scheme is also changed as follows: 1) all scan flip-flops are set to the test mode, 2) shift cycles are to load test signals, where is the length of the scan segments; and 3) the scan flip-flops are all set to the functional mode to receive the test responses. This is quite different from the test scheme of the original scan architecture that inserts one capture cycle after shift cycles (is the length of the original scan chains).

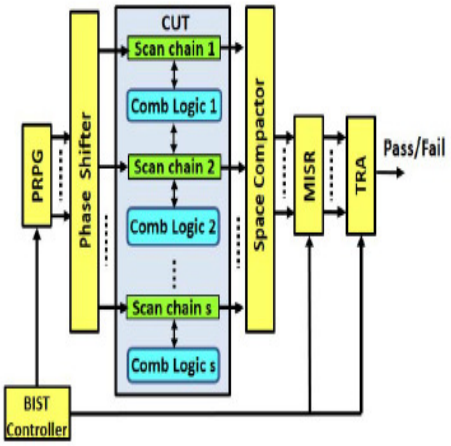
As stated above, a scan-in signal drives a number of scan segments by an exclusive-or of the scan-in signal and the test responses captured in the preceding scan segment. This may produce some extra signal correlation and some additional redundant faults in some cases if the scan flip-flops are not grouped properly. Outputs of all scan segments are connected with an XOR tree, which may cause some aliased faults. The scan flip-flop grouping scheme also influences testability of the

circuit. Our method tries to group scan flip-flops to avoid the aforementioned negative impacts while driving multiple scan segments with the same scan-in signal and connecting outputs of multiple scan segments to the same XOR tree. Merging two scan flip-flops does not generate any new convergent fan-out if they do not have any common successor in the combinational part of the circuit. Therefore, the test data fed to the scan segments of the same scan chain should have no correlation. This mainly benefits from the single stuck-at fault model that we are considering in our paper. It is also good for other fault models, such as, transition faults, path delay faults and multiple stuck-at faults. Any match of output flip-flop in each gathering don't have any basic forerunner in the combinational piece of the circuit with the end goal to abstain from associating. The test reactions lose no data due to the XOR trees if all sweep flip-flop in every one of the above output flip-flop bunches don't have any basic ancestors.

Test length of output based BIST is typically dictated by the irregular safe flaws. Test length decrease of the irregular safe deficiencies ought to be a vital issue. Different strategies are embraced to deal with the issue. In any case, a test vector is first moved into the sweep chains in test-per-filter BIST plot, and a useful cycle is embraced to catch test reactions after that. The test reactions caught in the output flip-flops are moved out when the following test vector is examined in. Dissimilar to the test-per-clock conspire, information contributions of all sweep flip-flops can't be seen amid the move cycles utilizing the test-per-filter BIST plot.

IV. EXISTED SYSTEM

The above figure (1) shows the architecture of existed system. In this paper, a versatile methodology is acquainted with decrease PD amid catch periods of sweep based LBIST, therefore diminishing the likelihood to create false test fizzles amid test. Like the arrangements, our methodology decreases the AF of the CUT contrasted and ordinary output based LBIST, by appropriately changing the test vectors produced by the Linear Feedback Shift Register (LFSR). Our methodology is by one way or another like reseeding systems to the degree that the succession of test vectors is appropriately changed with the end goal to satisfy a given necessity that, notwithstanding, isn't to expand FC (as it is typically the situation for reseeding), however to diminish PD. The essential thought behind our methodology (in its non-versatile adaptation) was presented.



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In our existed adaptable methodology, (at least one) test vector(s) to be connected to the CUT by ordinary sweep based LBIST is (are) supplanted by new, appropriate test vector(s), hereinafter alluded to as substitute test (ST) vector(s). The ST vector(s) is (are) produced dependent on the test vectors to be connected at past and future catch stages with the end goal to diminish the most extreme number of changes between any two after test vectors. Along these lines, the CUT AF and PD are decreased contrasted and the first test grouping. We think about the nearness of a stage shifter (PS), which is normally received in output based LBIST to lessen the relationship among the test vectors connected to contiguous sweep chains. All test vectors to be connected at past and future catch stages to any sweep chain are generally given at appropriate yields of the PS, or the PS can be effectively changed to give them.

In our methodology, this property is abused to empower its ease equipment execution. In any case, our methodology can likewise be embraced if the PS does not give the past and future test vectors for all output chains or if the sweep based LBIST does not present a PS. Our methodology is adaptable in the reachable PD decrease. Thusly, test designers could pick the correct AF with the end goal to keep away from the accompanying:

1) Faulty chips being tried as great (because of an actuated too low AF, lower than that accomplished amid ordinary activity);

2) Good chips being tried as defective (due to a prompted intemperate AF, higher than that accomplished amid ordinary activity).

PD adaptability is gotten by scaling the quantity of ST vectors to be connected between unique test vectors. , our answer requires generously less test vectors (therefore TT) to accomplish an objective FC contrasted and the elective arrangements, yet this framework doesn't gives compelling outcomes. So a new system is proposed which is discussed in below section.

V. PROPOSED SYSTEM

The below figure (2) shows the architecture of proposed system. Fundamentally, a test-per-scan BIST conspire is utilized in the STUMPS design. Since the quantity of valuable examples is known to be a little division of all created examples, a lot of vitality is as yet squandered in the LFSR. Further, test-vector reordering in a pseudorandom testing condition is a testing errand. To appraise vitality misfortune, we figure the aggregate SA as the quantity of 0 →□1 and 1 →□0 changes in all the circuit hubs including the LFSR, CUT, and the sweep way over an entire test session.

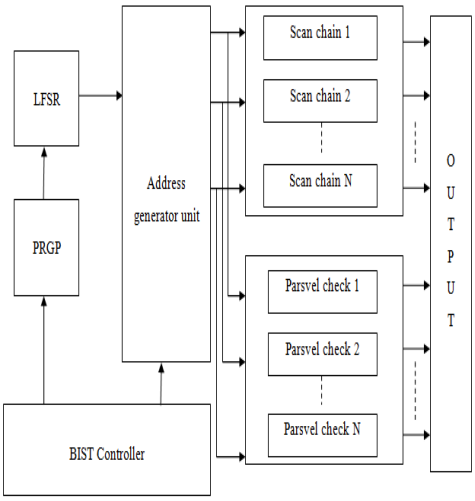

FIG. 2: PROPOSED SYSTEM

The different steps of the proposed technique are presently condensed beneath:

(i) A pseudorandom test succession is produced by a LFSR, and its single stuck to blame inclusion in the CUT is resolved through forward and invert blame

reenactment; let Sdenote the test arrangement up to the last helpful vector (past which blame inclusion doesnot enhance fundamentally).
(ii) For every arranged match of test vectors in the decreased set Sr = (S \ U), decide the exchanging movement (SA) in the sweep way and the CUT.
(iii) Reorder the vectors in Sr to appraise an ideal request S□ to limit vitality.
(V) Modify the state table of the LFSR with the end goal that it creates the new grouping S□.

The accompanying case of a TPG represents state skipping method. Henceforth, SA can be spoken to as a coordinated finish diagram called action chart, where every hub speaks to a test vector, and the coordinated edge (eij) speaks to use of the arranged test combine (ti, tj). The inherent part being free of test requesting is spoken to as a hub weight and might be overlooked the extent that the ideal requesting is concerned. The edge weights are spoken to as an unbalanced cost grid, as the variable segment of SA unequivocally relies upon requesting of test sets. In this way, for the test grouping S (t1→ t2 → t3 → t4 → t5), the variable segment of exchanging movement is 37. An ideal requesting of test vectors that limits the vitality utilization is a min-cost Hamiltonian way: S□ (t1→t2 → t5 → t4), the way cost being equivalent to 23. Since these extra changes exude just from the end request to keep the SA from happening in ML for each output move cycle, an empower flag E controlled by M is utilized. Subsequently, the y-inputs end up noticeable to ML if and just if M = 1. The test session ends when the end-condition of the last helpful example in S□ is come to. Assurance of ideal reordering of test designs is proportional to taking care of a traveling salesman problem (TSP), which being NP-hard, needs heuristic procedures for speedy arrangement.

VI. RESULTS

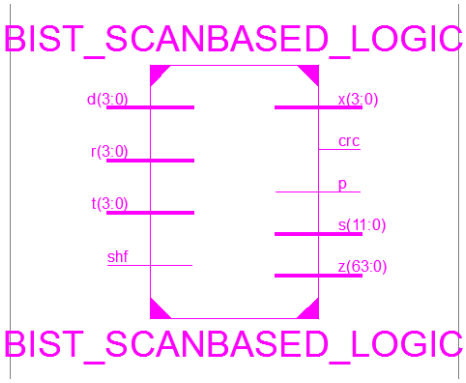

FIG. 3: RTL SCHEMATIC

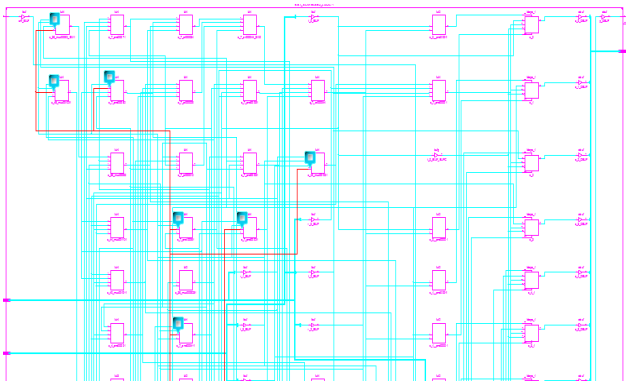

FIG. 4: TECHNOLOGY SCHEMATIC

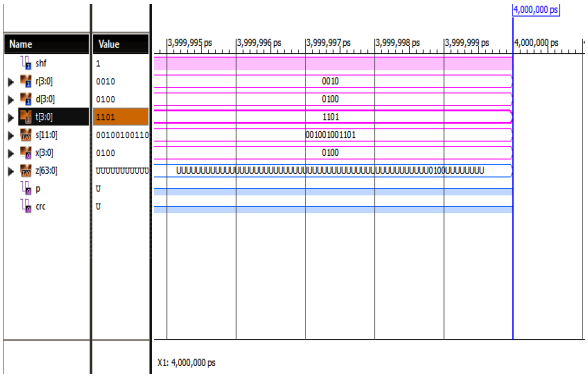

FIG. 5: OUTPUT WAVEFORM

B Project Status (11/30/2018 - 12:34:59)			
Project File:	ET3.xise	Parser Errors:	X 4 Errors
Module Name:	BIST_SCANBASED_LOGIC	Implementation State:	Synthesized
Target Device:	xc3s100e-5vq100	•Errors:	No Errors
Product Version:	ISE 14.7	•Warnings:	79 Warnings (79 new)
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	75	960	7%
Number of Slice Flip Flops	56	1920	2%
Number of 4 input LUTs	131	1920	6%
Number of bonded IOBs	94	66	142%
Number of GCLKs	2	24	8%

Detailed Reports					[-]
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri 30. Nov 12:34:57 2018	0	79 Warnings (79 new)	2 Infos (2 new)

FIG. 6: REPORT

VII. CONCLUSION

We have presented a novel approach to reduce PD during at speed test of sequential circuits with scan-based LBIST using the LOC scheme. The proposed solution enables designers to reduce the probability during at-speed test interpreted as a delay fault, with consequent generation of a false test fail. This is accomplished by diminishing the AF of the CUT contrasted and traditional output based LBIST.Compared to existed system, the proposed system gives effective results in terms of power consumption, speed and delay.

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