VLSI DESIGN OF BER MEASUREMENT FOR WIRELESS COMMUNICATION SYSTEM

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ABSTRACT: This paper presents the Bit Error Rate (BER) performance of the wireless communication system. The complexity of modern wireless communication system are increasing at fast pace. It becomes challenging to design the hardware of wireless system. The proposed system consists of MIMO (Multiple Input Multiple Output) transmitter and MIMO receiver along with the along with a realistic fading channel. To make the data transmission more secure when the data are passed into channel Crypto-System with Embedded Error Control (CSEEC) is used. The system supports data security and reliability using forward error correction codes (FEC). Each evolution of wireless communication system demands ever increasing growth in the rate of data transmission with no sign of pause. The demand of higher data-rate, exhibited by increasing users of mobile wireless services, has been on an exponential path. To meet such requirement of data-rate, wireless industry has already specified to further augment data rates up to 3 Gbps milestone for next generation wireless communication systems.

Keywords: Crypto-System, FEC codes, BER.

I. INTRODUCTION

Monte Carlo (MC) simulation techniques have been widely used to generate BER versus a range of expected signal-to noise ratio (SNR) conditions. However, the execution times of software-based MC simulations of the baseband layer on workstations can be extremely long, especially for increasingly complex communication systems. Bit error rate (BER) characteristic is one of the basic measures of the performance of any digital communication system.

Bit error rate (BER) is the ratio of the number of incorrect to the total number of received bits. The proposed BER measurement system consists of transmitter and receiver. The proposed wireless communication system consists of transmitter and receiver. The transmitter part consists of encoder, inter-leaver and modulator. The receiver part consists of ML detector, de-inter-leaver and decoder. There are two modes of operation in inter-leaver Read after write at the transmitter side and Write after read at the receiver side.

Linear Feedback Shift Register (LFSR) is used to generate the PN sequence. To make the transmitted data more secure encryption and decryption process are followed. A Linear Feedback Shift Register (LFSR) is a shift register whose input bit is a linear function of its previous state. LFSR is used to generate PN sequence.

Inter leaver is an essential part and is also responsible for an excellent BER performance of turbo code. Inter leaver architectures are well studied in literature.

Systematic procedure of building wireless-communication test-environment is an essential step for the verification of such hardware prototypes. However, hardware implementation of entire communication system consumes huge amount of time and is expensive procedure. Nevertheless, significant blocks of such communication system can be implemented on real-

hardware (FPGAs/ASIC) and rest can be designed on software platform. Thereby, integrating such software test-environment of the communication system with decoder hardware-prototype can verify its functionality. It is essential to compare the decoder BER-performance that is obtained from simulation in software platform with the performance of hardware-implemented decoder.

High-throughput and energy-efficient design of turbo decoder is an important object of interest in the wireless industry at present. These are two serious bottlenecks of present-day turbo-decoder architectures which might be obsolete from the next generation wireless communication standards unless such issues are resolved. Thereby, this thesis has adapted progressive methodology of solving such recent challenges. In this work, we have studied the behavior of turbo code in a wireless communication environment and analyzed the performance under various conditions.

II. LITERATURE SURVEY

1. Inter leaver and De-inter leaver

The basic function of an inter leaver is to protect the transmitted data from burst errors. The inter leaver spreads these time bits out in time so that all these bits are not corrupted at the same time by the deep fade or noise burst. In the inter leaver, a 14-bit counter is used to write the coded input bits into a 16 384×1 memory. This counter counts linearly from 1 to 16 383 and goes back to 1. At the output, a 14-bit LFSR is used to read out the coded bits randomly from the memory to decrease the correlation between the encoded samples.

In the de-inter leaver, the reverse operation is performed, where the received bits are written randomly into a memory using the same pseudorandom sequence and later read out using a circular counter.

- We propose a modified MAP-decoder architecture based on a new un-grouped backward recursion scheme for the sliding window technique of LBCJR (logarithmic Bahl –Cocke –Jelinek –Raviv) algorithm and a new state metric normalization technique. The suggested techniques have made provisions for retiming and deep pipelining in the architectures of SMCU (state-metric-computation-unit) and MAP decoder, respectively, to speed up the decoding process.

- Subsequently, the fixed point simulation for BER performance analysis of parallel turbo decoder is carried out for various iterations, quantization and code rates.

2. Decoder Architectures and Scheduling

This section presents MAP-decoder architecture and its scheduling based on the proposed techniques. We have further discussed design and implementation-trade-offs of high-speed MAP-decoder architecture. Then, parallel turbo-decoder architecture and inter leaver used in this work are presented.

FPGAs (field programmable gate array) are powerful programmable logic devices and have recently become very popular. The gate count per FPGA chip has increased considerably over the last few years. The re-programmable feature of FPGAs is provided by static RAM technology. FPGAs are customized by loading configuration data into internal memory cells. The configuration data can be thought of as a single instruction which the FPGA executes each time.

III. PROPOSED SYSTEM

Below figure (1) shows the design and implementation of PRPG based encoder and decoder. The flow chart consists of the following input, pre-permutation, Inter leaver, parallel to serial, encoder output, serial to parallel, De-inter leaver, PRNG and finally the output in detailed manner.

A Linear Feedback Shift Register (LFSR) is a shift register whose input bit is a linear function of its previous state. LFSR is used to generate PN sequence.

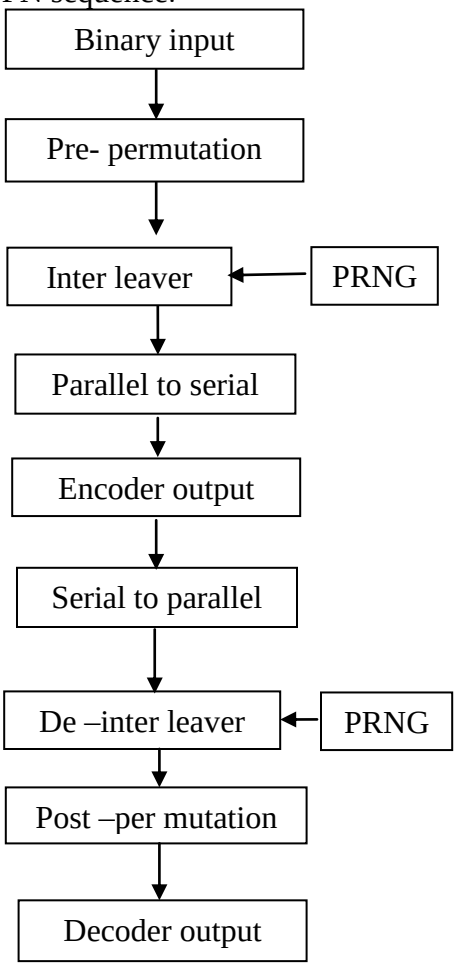

FIG. 1: DESIGN AND IMPLEMENTATION OF PRPG BASED ENCODER AND DECODER

Consider two independent normally-distributed variants with zero means and equal variance. To implement a Rayleigh fading variant generator, Without generating two Gaussian variables p and q we can compute the magnitude of the complex Gaussian-distributed variant. According to the BM algorithm, if there are two independent uniformly -distributed pseudorandom numbers (PNs) in the interval (0, 1) and, then and two independent variants from a zero-mean, u with Gaussian distribution N (0,1), it follows Rayleigh distribution. To implement a Rayleigh variant generator, using two independent Gaussian variables, and then computing the magnitude of the complex Gaussian-distributed variant.

The first step of the decryption is to identify the exact positions of the deleted data for the decoding algorithm. It is not necessary to decrypt previous blocks successfully. However, it is necessary to be synchronized with the encryption process to maintain the right system state in terms of the permutation arrays and the PRNG state.

IV. SIMULATION RESULTS

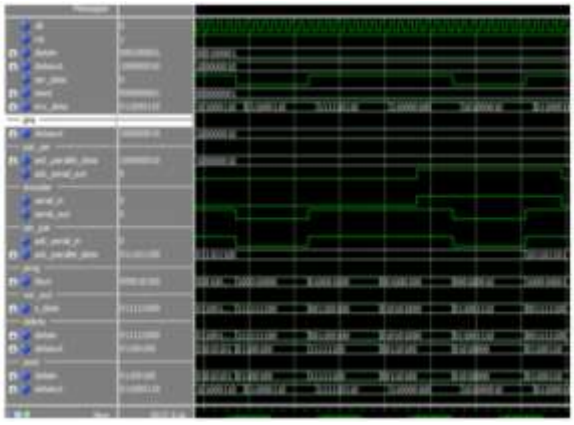

Fig. 2: ENCRYPTION OUTPUT

To encrypt, start by permuting the bits of the input block using the permutation array. The encoded block is randomized by XOR it with the random sequence from PRNG. (Pseudo -random number generator)is generated by using the LFSR. This is followed by the delete step where out of the columns are selected and removed from the

randomized block. After deletion post-permutation operation is performed.

FIG. 3: TRANSMITTER OUTPUT

In the above figure 3 the encrypted input is given as the input to the transmitter.8 bit of encrypted data is given as the input to the encoder after encoding they are interleaved .To avoid the data loss while the transmission is going they are loaded into the memory. The interleaved data are modulated using the BPSK modulator and the modulated is transmitted using the local oscillator. After when the data are passed into the channel it will be various like noise and Rayleigh fading.

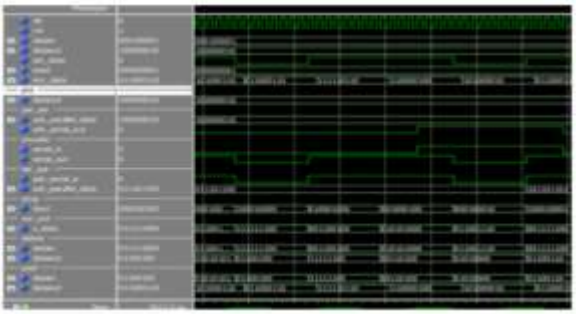

FIG. 4: DECRYPTION OUTPUT

To decode the transmitted data which being transmitted data same set of PN sequences are generated at receiver side and the encrypted data are decrypted by following the same steps which are followed at receiver end to decode the data which are being transmitted. After performing the decoding process Bit error rate is measured.

V. CONCLUSION

In this paper Wireless communication system is designed using VDHL. To make the data transmission more secure when the data are passed into channel Crypto-System with Embedded Error Control (CSEEC) is used. In the recent years, high-throughput design and implementation have become dominating requirement in the field of VLSI design of wireless-communication systems. There has been a rapid surge in data-rate for next-generation wireless-communication and this will lead to more complex algorithms and VLSI architectures in next few decades. Based on this scenario, we have aggregated the study of turbo-code and the design of high-throughput parallel-turbo decoder in this thesis. To this end, we have realized the importance of understanding an algorithm in real-world scenario and then realizing application-specific architecture for it. Thereby, it is essential to explore both algorithmic as well as architectural sides of wireless-communication system to conceive a best design that meets the requirement of next-generation technology.

VI. REFERENCES

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