Implementation of Brent Kung Carry Select Adder Using Routing Technique

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Abstract

In the Digital world, adders are essential in any VLSI architecture and processors as it is the basic unit. Now the thing that matters is the performance of adder. Carry Select Adder (CSLA) is one of the type of fastest adders used for high speed arithmetic operations to alleviate the problem of carry propagation delay. CSLA architecture is proposed using parallel prefix adder. CSLA is a compromise between small area but longer delay Ripple Carry Adder (RCA) and larger area with shorter delay Carry Look Ahead Adder in term of area and delay. Delay of RCA is large therefore, it is replaced with parallel prefix adder which gives fast results. In this paper, a VLSI architecture of carry select adder using Brent Kung Adder is proposed and a different routing technique is used to design an area effective adder. The proposed architecture is designed and simulated in Vivadov2017.2 software.

Keywords: Brent Kung Adder (BKA), Ripple Carry Adder (RCA), Full adder (FA), Carry Select Adder (CSLA), Parallel prefix adder, Area and Power.

1. Introduction

In present market, growth of portable electronic component have rapidly increased the demand for low power arithmetic circuits in VLSI industry. Multiplier-Accumulator (MAC) unit is the main building block in DSP processor. Adders significantly affect the efficiency of whole system as they are the part of MAC unit [1]. Adder is a digital circuit which performs not only addition of numbers, but also subtractions, multiplication and division. The Addition is one of the basic need for a multiplication. Hence, it is an integral part of ALU. These are found in most of the microprocessors and microcontrollers, adders are frequently used for executing many instructions. The reduction of power consumption of FA circuit is necessary for low power application. Fast and accurate operation of digital system depends on the performance of adder. The operation of an adder is limited by the carry propagation signal because the generation of a signal requires a more amount of time when compared with the summation output. There are different types of adders but they are used depending upon area, speed and accuracy.

Ripple Carry Adder (RCA) is the simplest digital circuit that produces the arithmetic output sum and carry-out of two binary numbers. The RCA is constructed by cascading FA blocks in series. A one-bit full adder adds three one-bit numbers. RCA provides the most compact design but takes longer computing time as carry-out of one stage is fed directly to the carry-in of the next stage 4-Bit RCA. A major drawback of this adder is that the delay increases linearly with the bit length [1].

In order to improve the drawbacks of RCA i.e., to remove the linear dependency between computation delay time and input word length, Carry Select Adder (CSLA) is mostly used. The basic CSLA architecture consists of two RCA and a multiplexer. The CSLA is simple but rather fast, having a gate level depth of O (sqrt n) [2]. The CSLA is used to alleviate the problem of Carry Propagation Delay (CPD) by independently generating multiple carries and then select a carry to generate the sum by using multiplexer. As it uses multiple pairs of RCA for generating partial sum and carry-out, it is an area inefficient [3].

2. Parallel Prefix Adder

Parallel Prefix Adders [4] are one of the unique adders that are used for high performance arithmetic circuits in industries as they increase the speed of operation. In order to obtain a parallel prefix adder , a Carry Look Ahead Adder is utilized. Tree structure algorithm are used to increase the speed of arithmetic operation [5]. There are three stages to obtain a parallel prefix adder and they are :

1. Pre- processing stage
2. Carry generation stage
3. Post processing stage

2.1. Pre-processing Stage

In this stage, generate and propagate signals are computed for both the inputs A and B .These signals are given by the following equations [6]:

$$P(i) = Ai \text{ ^ } Bi \quad (1)$$

$$G(i) = Ai \,.\, Bi \quad (2)$$

For all i= 0, 1, 2,… n-1 where n is no. of bits and Where '^' and '.'indicates XOR and AND operation respectively.

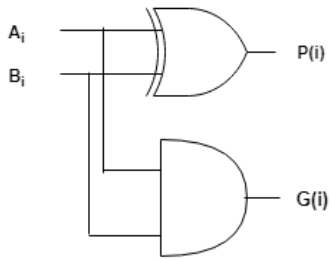

Figure 1. Pre-processing stage

2.2. Carry Generation Stage

In this stage, all the operations are implemented and carried out in parallel. Carry propagate and generate signals are used as intermediate signals in this stage which are given by the following logic equations:

$$G1 = G(1) + \big(P(1).G(0)\big) \quad (3)$$

$$P1 = P(1).P(0) \quad (4)$$

$$Pi = P(i).Pi - 1 \quad (5)$$

$$Gi = G(i) + (P(i).Gi - 1) \quad (6)$$

For all i= 2,3,…n-1 where n is no. of bits and where '+' and '.' Indicates OR and AND operation respectively.

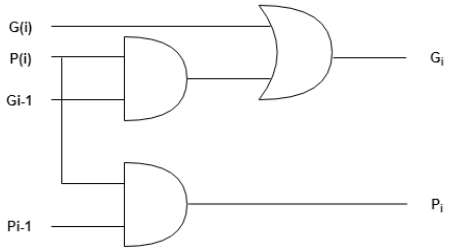

Figure 2. Carry Generation Stage

Carries of each input bit is given by equations:

$$C0 = G(0) \quad (7)$$

$$Ci = Gi \quad (8)$$

for i=1,2…n-1 where n is no. of input bits.

2.3. Post processing Stage

This is the final stage to compute the summation of input bits. It is the last stage of parallel prefix adder. It is similar for all the adders and then sum bits are computed by logic equation:

$$S(0) = P(0) \quad (9)$$

$$S1 = P(1)\text{^}G(0) \quad (10)$$

$$Si = P(i)\text{^}Gi - 1 \quad (11)$$

$$Cout = Gn - 1 \quad (12)$$

for i=2, 3,… n-1 where n is no. of bits and where '^' indicates XOR operation.

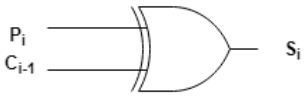

Figure 3. Post processing stage

3. Brent Kung Adder

Brent Kung Adder [4] is one of the parallel prefix adder, which perform high-speed binary arithmetic operations .These adders are the ultimate class of adders that are based on the use of generate and propagate signals. It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. In Brent Kung adders along with the cost, the wiring complexity is also less. But the gate level depth of Brent-Kung adders is O(log2 (n)), so the speed is lower.[5]

4. Regular Linear Brent Kung Carry Select Adder

. Conventional CSLA consists of a pair of RCA and a multiplexer. Brent Kung Adder (BKA) is a type of parallel prefix adder. BKA has reduced delay compared to RCA

as the internal operation of BKA is operated parallelly i.e., tree structure is used. So Modified CSLA using BKA is designed. The Modified CSLA using BKA of 16 bit consists of a RCA, BKA and a multiplexer. When compared with the CSLA, one RCA is replaced with BKA for carry-in='zero', hence delay will be reduced as BKA is one of parallel prefix adder. Here there are two groups
Group1 contains only a 4-bit BKA with carry-in='zero' and sum and carry-out are pre-evaluated. Group2 contains a 4-bit RCA with carry-in='one' and a 4-bit BKA with carry-in='one' and here also sum and carry-out are pre-evaluated. The carry of group1 is fed to MUX to select the output sum and carry-out of group2 and this pattern continues in similar manner for upcoming stages. The RCA requires a more number of transistors for the implementation of the adder logic i.e,, if the width size is increased the number of full adders are also increased proportionally. But BKA adder requires a less number of logic gates to implement the same logic and as BKA uses parallel operation, the BKA adder has less delay and more area efficient.[5]

5. Proposed Methodology

In this paper, the proposed architecture contains a Brent Kung Adder (BKA), Ripple Carry Addition (RCA) and a Multiplexer (MUX). RCA is the most compact full adder but its performance is limited by a carry that must propagate from the least significant bit to the most significant bit.

The modified Brent Kung adder is divided into groups. Group1 contains 2–bit BKA, which adds the input bits and the carry-in and gives result and the carry-out. The group2 contains 2-bit BKA for carry in='zero' and 2-bit RCA for carry-in='one' and a MUX. The carry out of group1 is used as selection input line to MUX which is in group2, selects the result from the corresponding BKA for carry-in= 'zero' and modified RCA for carry-in='one'. Similarly, the remaining groups will be selected depending on the carry-out from the previous groups. For both RCA and BKA, routing is modified to decrease delay and power consumption. The following are the proposed sum and carry out equations for 2-bit RCA:

$$s = a\hat{}b\hat{}cin = a\hat{}b\hat{}1 = a\hat{}\sim b \quad (10)$$

$$c = a.b + b.cin + cin.a = a + b \quad (11)$$

(Since the value of cin='one'.)
Where a, b and cin='one' are inputs and s and c are the output sum and carry-out of 2-bit RCA respectively.

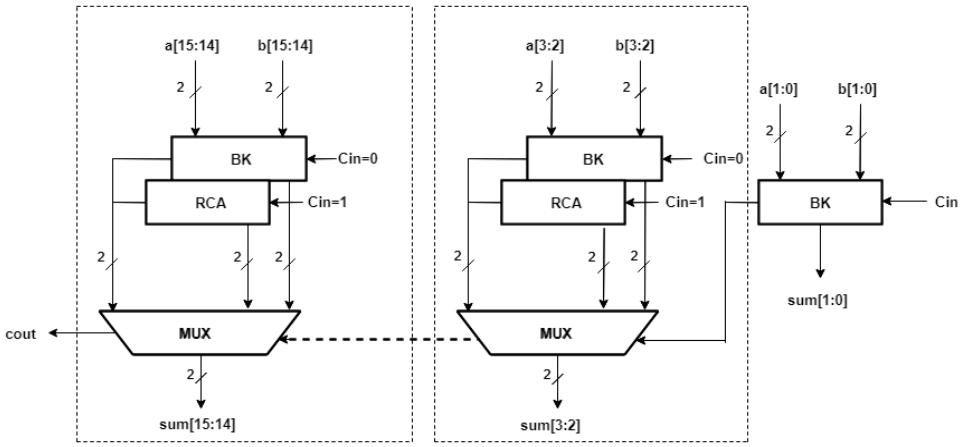

Figure 4.Schematic diagram for Carry Select Adder using Brent Kung adder

The transistor count in the proposed architecture is reduced due to routing. Here a RCA and BKA of different routing is used, so the equations have been reduced as shown in equation (10) and (11) and the number of gates are also decreased. Therefore, the proposed methodology is an area efficient and less power consumption adder.

6. Simulation Results

The simulated results for Kogge Stone Adder using Binary to Excess one Converter (KSA BEC) and Brent Kung Carry Select Adder (BK CSLA) are as shown in Fig.5 and Fig.6 respectively.

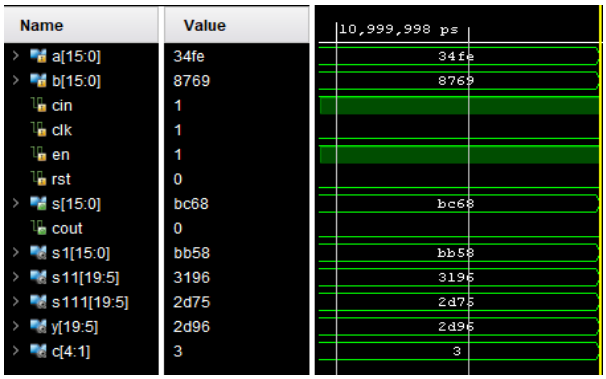

Figure 5. Simulated result for Kogge Stone Adder using Binary to Excess one Converter

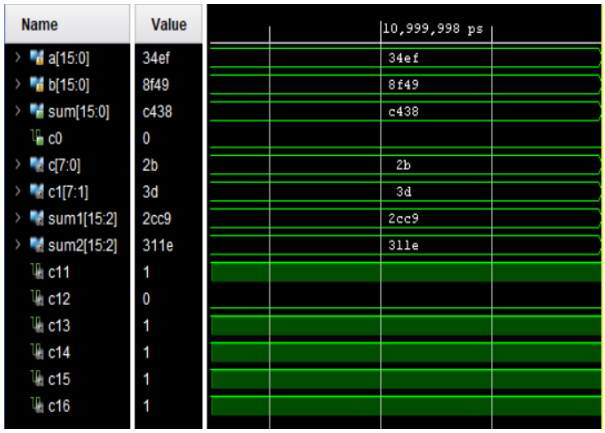

Figure 6. Simulated result for Carry Select Adder using Brent Kung

6.1. LUT COMPARISON

For lower bits, there is no considerable change in number of LUTS. But as the bit size increases the number of LUTS decreases when compared to regular CSLA. So modified CSLA using BKA is more efficient for higher bit size.

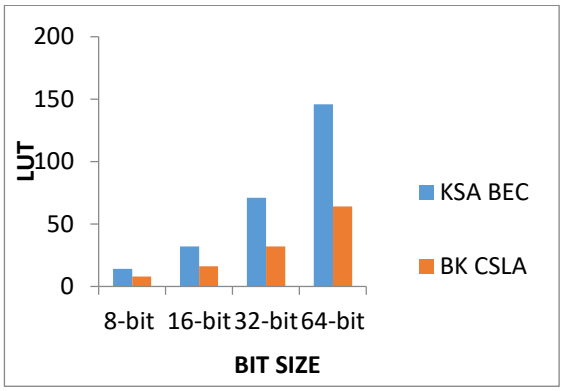

Figure 7. Comparison of LUT of different bit size

Table 1. Comparison of Area in terms of LUTS

NUMBER OF LUTS				
Adders	8-bit	16-bit	32-bit	64-bit
KSA – BEC	14	32	71	146
BK CSLA	8	16	32	64

6.2. POWER COMPARISON

In practical world, most of the electronic devices perform complex computation, so large bit sizes are in demand. For lower bits, there are only minute changes in total power (i.e., static and dynamic power). As the size of the bit increases, the total power consumed gets decreased when compared to KSA BEC

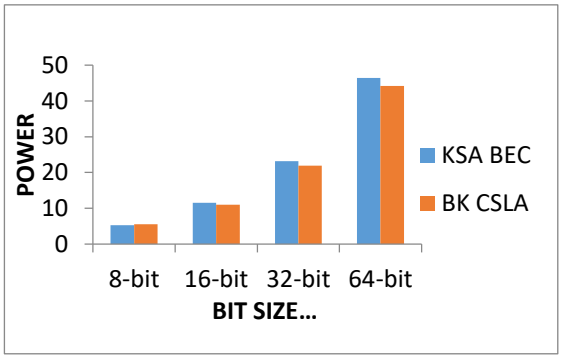

Figure 8. Comparison of POWER (in w) for different data bits

Table 2. Comparison of POWER for different adders

POWER IN WATTS				
Adders	8-bit	16-bit	32-bit	64-bit
KSA BEC	5.308	11.563	23.129	40.441
BK CSLA	5.559	11.014	21.96	44.157

7. Conclusion

Design of a Brent Kung Carry Select Adder is proposed in this paper, which is obtained by changing the routing of CSLA. In FIR, IIR filters and FFT algorithms, the things that matter are area ,speed and power consumption, so the basic adder unit must not compromise in any of the former parameters. By using parallel prefix adder, area and power consumption of different adder architectures is reduced. As Parallel Prefix Adders are one of the fastest adder and they derive fast results, BKA is used. The transistor count gets reduced. From the results, it is concluded that the power consumption of proposed model is decreased nearly by 5 percent and area get reduced when compared to regular linear Kogge Stone Adder using Binary to Excess one Converter.

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9. References

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