Design of Reconfigurable Coefficients Driven FIR Filter using Modified Radix-4 Booth Multiplier and Modified Kogge-Stone Based Carry Select Adder

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Abstract

In cellular communication and multimedia applications, there is need for high speed ,low power and low cost filters, here Reconfigurable Finite Impulse Response (RFIR) filter can fulfil these requirements. In this paper, the work is mainly concentrated on enhancing multiplier, adder structures of the filter and also usage of the Reconfigurable coefficients. Radix-4 Booth multiplier, Kogge-Stone based carry select adder structures are used in this paper. A reconfigurable coefficient reduces some accuracy but it eventually leads to the stunning performance in FIR filter response parameters like in its power, speed and area. Initial work is carried out by coding the designs in Verilog HDL later the synthesis and simulation is carried out in MATLAB 2017b Simulink software along with VIVADO v2017.2 using Xilinx System Generator.

Keywords: Booth multiplier**,** FIR filter, Kogge stone based carry select adder,Radix-4,Reconfigurable coefficients

1. Introduction

The ever increasing growth in laptop and portable systems in cellular networks has intensified the research efforts in low power microelectronics. Today, there are numerous portable applications requiring low power and high throughput than ever before. For example: notebook, laptop's and computers representing the fastest growing segment of the computer industry, are demanding the same computation capabilities as found in desktop machines. Equally demanding are developments in personal communication services (PCS's), such as the current generation of digital cellular telephony networks which employ complex speech compression algorithms and sophisticated radio modems in a pocket sized device. Thus, low power system design has become a significant performance goal. So designers are faced with more constraints: high speed, high throughput, less silicon area, and at the same time, consumes as minimal power as possible.

Digital FIR filter is popularly used in Signal Processing for noise removal and related applications. Signal processing and filtering are the two most frequent operation in many biomedical applications, instrumentation, speech and audio processing, data communication and robotics. FIR digital filters are widely used in digital signal processing by virtue of stability and easy implementation FIR filters are said to be finite because they do not have any feedback[1].
Fir filter gives output through the convolution of its filter coefficients and input sequences.

$$\mathbf{Y[}n\mathbf{]=}X\mathbf{[}n\mathbf{]}*H\mathbf{[}n\mathbf{]} \quad (1)$$

For nth order FIR filter, resultant signal of the filter is weighted function of the latter values of the input signal.

$$y(n) = \sum_{p=0}^{N-1} h(p)x(n-p) = \sum_{p=0}^{N-1} x(p)h(n-p) \quad (2)$$

Here, x(n) is the transmitted sequence, h(n) shows the coefficients of digital FIR filter and Y(n) is the obtained output of FIR filters . Here N represents order of the filter.

Thus, in this paper, a FIR filter is built, which is potent not only in terms of power and area, but also in terms of delay. When we consider the elementary structure of a FIR filter, we see that it is a combination of multipliers and delays, which are in turn the combination of adders. Thus, the adders serve as basic components in the implementation of a FIR filter. In addition, addition is one of the fundamental arithmetic operations widely used in many VLSI systems such as microprocessors and application-specific DSP architectures. In addition to his main function, namely the addition of two numbers, he participates in many other useful operations such as subtraction, multiplication, division, etc. The objective of the research is therefore to design an efficient low-power adder that can then be used to build multipliers, then FIR filters[2].

Programmable FIR filters are required in reconfigurable systems to provide flexibility to support a wide variety of applications, which is one of the major challenges in the IoT market and even different FIR kernels are often needed within the same application. In this scenario, different sets of coefficients defined by the various applications as well as their individual filter kernels and derived during design time of the (software) application are re-assigned at runtime to the programmable FIR filter[3-6].

In Booth multiplication, partial product generation depends upon the recoding scheme e.g. Radix-2 encoding. Multiplication using normal Booths recoding algorithm technique based on the partial product can be generated for a group of consecutive 0's and 1's which is called Booths recoding. This recoding algorithm is used to generate an efficient partial product. This increase in the width of partial product usually depends upon the radix scheme used for recoding.

The booth algorithm is an effective technique for 2s complement multiplication. The booth algorithm reduces the number of partial products by shifting over a string of zeros. The increase in speed is proportional to the number of zeroes in the recoded version of the multiplier. In this radix2 algorithm, the main disadvantage is no. of partial products increases when one of the inputs is alternatively 1's and 0's i.e.,01010101.

Kogge-Stone structure is very attractive for high-speed applications..It is one of the fastest parallel prefix adder obtained from carry look ahead structure with focus on design time and in common choice for high performance adders in industry. The parallel-prefix adder becomes more favourable in terms of speed due to the $O(\log_2 n)$ delay through the carry path compared to O(n) for the RCA. The cost of long wires that must be routed between stages. Despite these cost ,KSA is generally used for wide adders because it shows the lowest delay among other structures [7-8].

The paper is structured as follows. Section 2 describes about Conventional FIR filter structure. Section 3 Proposed reconfigurable fir filter design. Section 4 deals with the synthesis, simulation results. Finally, Section 5 concludes the work done.

2. Conventional FIR filter structure

FIR digital filters are widely used in digital signal processing by virtue of stability and easy implementation.FIR filters are said to be finite because they do not have any feedback. Conventional FIR filter structure has coefficient unit ,multiplier ,delay and adder structure as shown in Figure 1. Here X and c0,c1,..c15 are the inputs and coefficients respectively and Y is output for Conventional FIR filter.It has high power consumption and delay due to Ripple carry adder structure and normal multipliers.

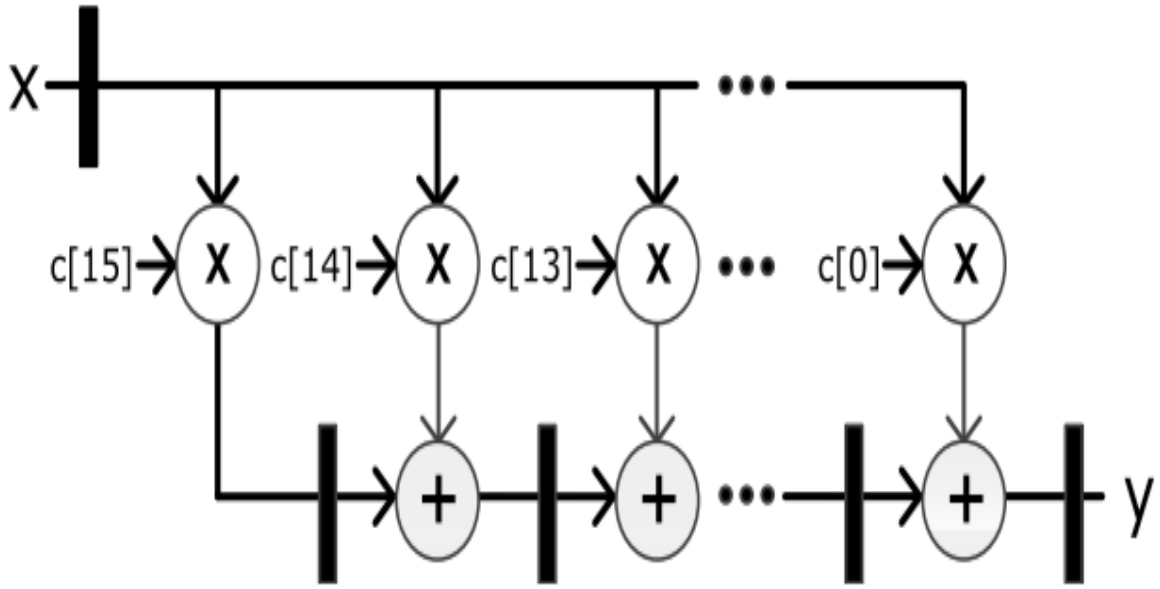

Figure 1. Conventional FIR filter

3. Proposed Reconfigurable FIR filter design

Proposed Reconfigurable FIR filter design is same as coventional structure but here mainly multiplier coefficients and adder structures are modified.In this proposed design uses reconfigurablecoefficients ,modified booth multiplier and kogg-stone adder structures are usedas shown in Figure 2. This proposed structure also simulated in MATLAB2017bsimulink obtained results by giving input sine wave with noise signal then converted to digital signal as shown in Figure 3.

In Reconfigurable coefficients block has inputs h0,h1,h2,....,h15 sixteen coefficients and outputs g0,g1,g2.....,g15 respectively.It changes the lower nibble to best nearest low value no of binary ones for each coefficient. Suppose lower nibble of one coefficient is '0111' then it changes to nearest low value which has less no of ones i.e.,'1000' Due to this accuracy of filter decreases but it made stunning performance in LUT's,power and speed.

This proposed structure has blocks like Radix 4 booth multiplier and kogge stone adder structure using multiplexer. Each block is explained below.

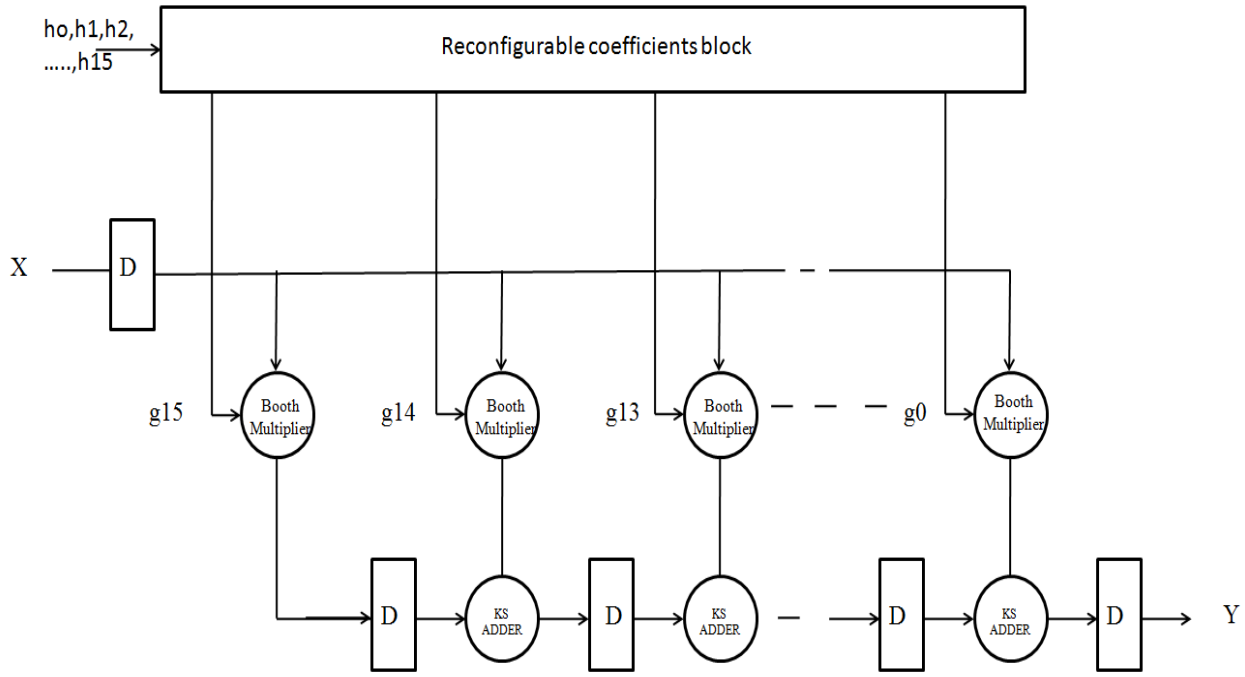

Figure 2.Reconfigurable FIR 16 tap filter structure

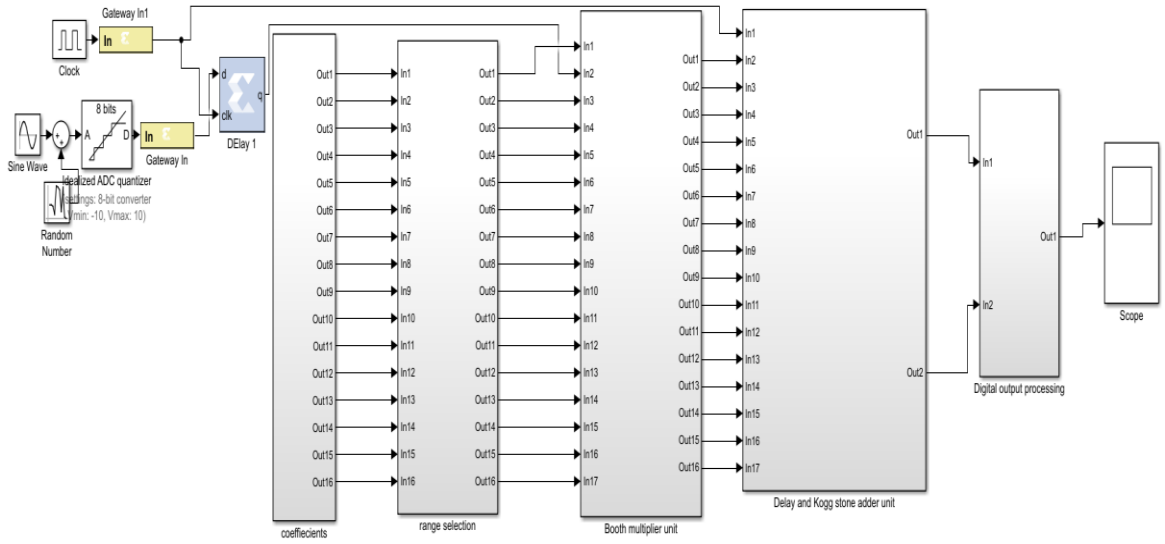

Figure 3. Block diagram for Reconfigurable FIR 16 tap filter simulinkstructure

3.1. Modified Radix 4 Booth multiplier using multiplexer:

In this Modified Radix 4 booth multiplier, n/2 stages and n/2 partial products exist, here n is input data length. Each stage consists three blocks such as 9-Bit multiplexer, 9-Bit adder/subtractor and code. Only in stage 1 in place of 9-Bit adder/subtractor block two more blocks namely 9-Bit mux binary to 2's compliment and 9-Bit mux 2:1 are placed as shown in Figure 4.Here inputs are 'X' and 'Y' which are 8 bit length and ouput has 16bit length represented with 'P'[9] .

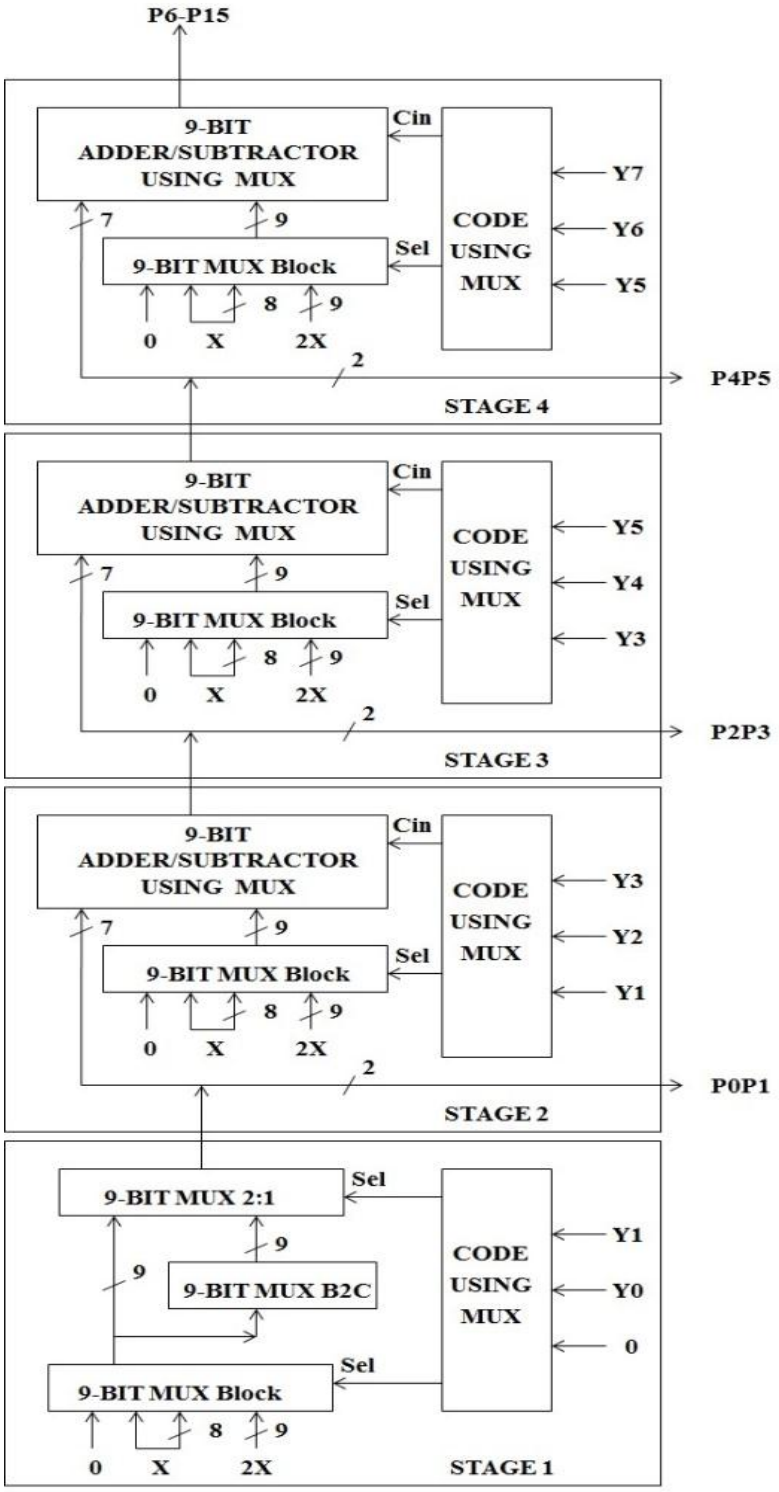

Figure 4. Modified Radix 4 booth multiplier using multiplexers

3.2. Modified Kogge-stone based carry select 16 bit adder using multiplexer

The structure of Modified kogge-stone based carry select 16 bit adder using multiplexer is shown in Figure 5.It has eight groups. Each group consist of 2 bit kogge stone adder (KSA) ,2Bit Kogge

stone adder with carry and three 2:1 multiplexer except first group which has single 2 bit KSA with carry only. In which we have Group1 consists of KSA 2 bit with carry c_{in} . Group 2 contains KSA 2 bit with and without carry with three 2:1 multiplexers. Similarly throughout group 8 . Depending upon the previous carry the selection of either one of the 2 bit KSA output is fed to the 2:1 multiplexer along with carry.If previous carry i.e., group1 carry is '0' then group 2 2Bit KSA block sum and carry is selected otherwise 2Bit KSA carry block outputs are selected same way till last group continues .

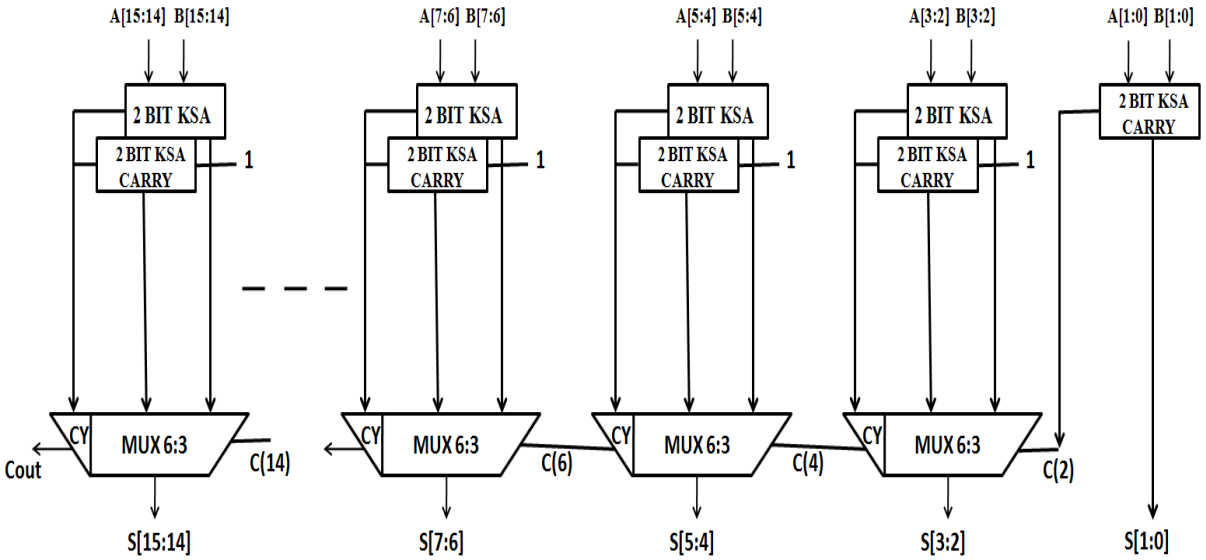

Figure 5.Modified Kogge stone based carry select 16 bit adder structure

3.2.1. Kogge stone 2Bit adder structure without carry

Multiplexer based 2BitKogge stone adder stucture consists of three NOT gates,one AND gate and four 2:1 multiplexers as shown in Figure .6. Here inputs are 'A[0]' ,'A[1]','B[0]' and 'B[1]' respectively and outputs are sum S[1:0] and carry C[2] respectively.

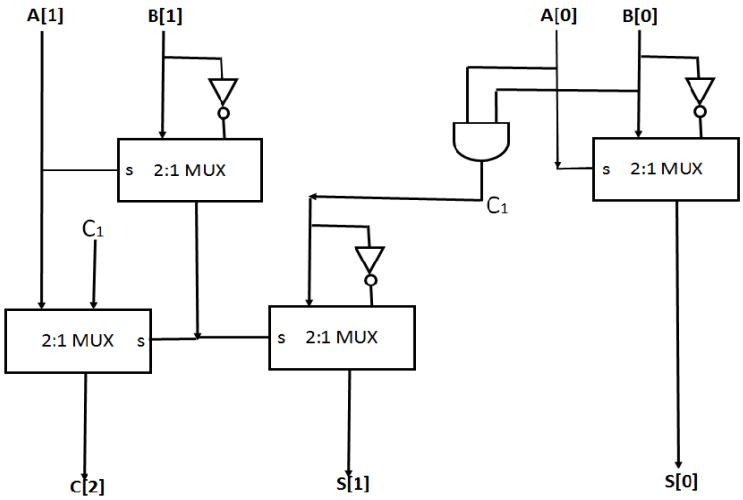

Figure 6.Kogge stone 2Bit adder structure without carry

3.2.2. Kogge stone 2Bit adder structure with carry

Multiplexer based 2BitKogge stone adder stucture as show in Figure .7.It consists of four NOT gates and six 2:1 multiplexers as shown in Figure .2. Here inputs are 'A[0]' ,'A[1]','B[0]' ,'B[1]' and Cin respectively and outputs are sum S[1:0] and carry C[2] respectively. Input Cinalways binary '1' value given throughout structure.

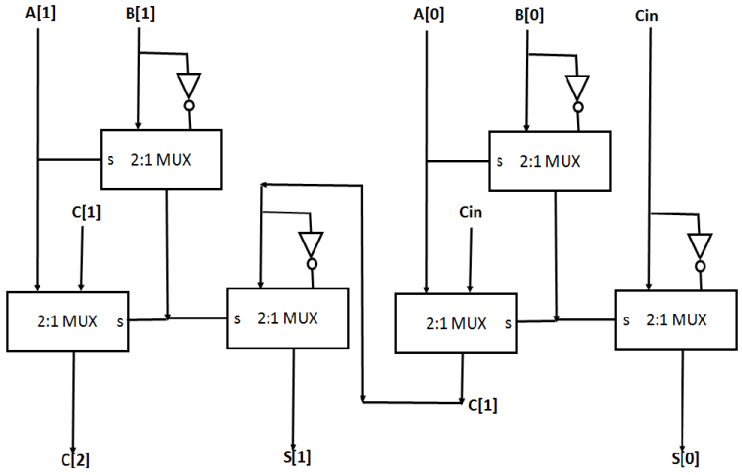

Figure 7.Kogge stone 2Bit adder structure with carry input

4. Results

The proposed methodology is simulated and synthesized on the Xilinx software in Vivado v2017.2 and also implemented on Matlab 2017b using system generator .The simulated resultfor 16 Tap Reconfigurable FIR filter using booth multiplier and kogg-stone adderis shown in Figure . 8.

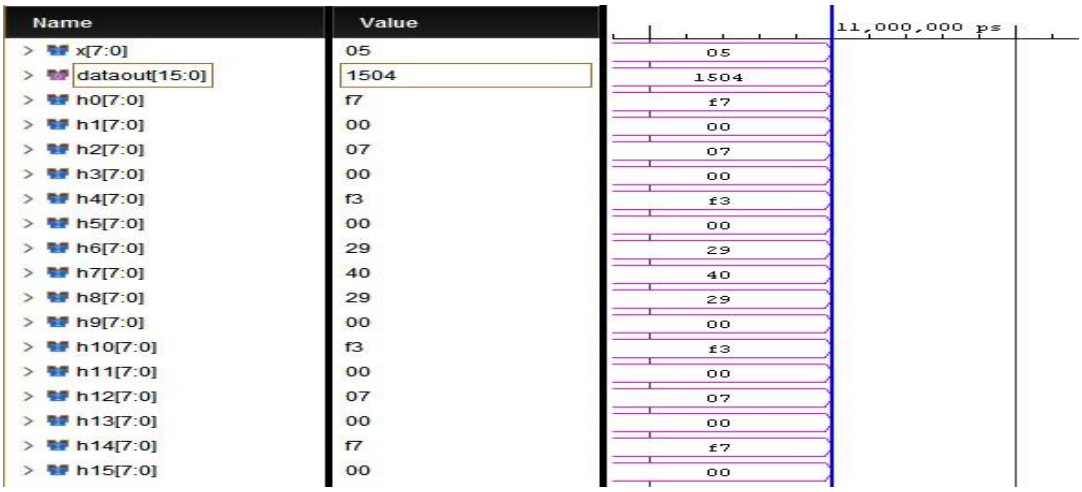

Figure . 8. Simulation result for 16 tap Reconfigurable FIR filter using radix 4 booth multiplier and kogge stone adder

Inputs for 16 Tap Reconfigurable FIR using booth multiplier and koggestone adder are x[7:0] taken as "00000101" and filter coefficients h0,h1,...h15 and so obtained output dataout[15:0] is "0001010100000100".

The proposed 8tap and 16tap Proposed Reconfigurable filter designs are coded in Verilog and the synthesis is carried out using Xilinx software in VIvado v2017.2. The net list file consists of the number of LUT's, delay and power consumption of respective designs are mentioned in TABLE 1. The proposed Reconfigurable FIR filter design has significant less delay, area and power consumption compared to conventional FIR are also shown in TABLE 1.

TABLE 1.FIR FILTERS COMPARISON IN LUT'S, DELAY AND POWER

S.NO	TYPE	8 Tap			16 Tap		
		LUT	POWER (w)	DELAY (ns)	LUT	POWER (w)	DELAY (ns)
1	Proposed Reconfigurable FIR filter design	120	13.521	9.605	276	18.617	26.133
2	Conventional FIR	186	18.343	11.479	366	23.548	28.351

The proposed Reconfigurable fir filter design using Booth multiplier and Kogge stone adder shows significant less delay, less area and power consumption compared to conventional fir design. The proposed 8 tap fir filter offers savings of 35.48%in area, 26.2%in power and 16.32% lesser delay than the conventional fir filter.similarly 16 tap fir filter offers savings of 24.59%in area, 20.94%in power and 7.8% lesser delay than the conventional FIR filter.

By using Booth multiplier and kogge stone adder structure in the FIR filter architecture maximum amount of reduction is observed in LUT's,power and delay of the design. for better understanding the the above results are depicated graphically and shown in Figure .9 and Figure .10 where as Figure .9 shows the LUT's,power and delay comparison of proposed 8 tap fir filter with conventional filter, Figure.10 shows the LUT's,power and delay comparision of proposed 16 tap fir filter with conventional fir filter.

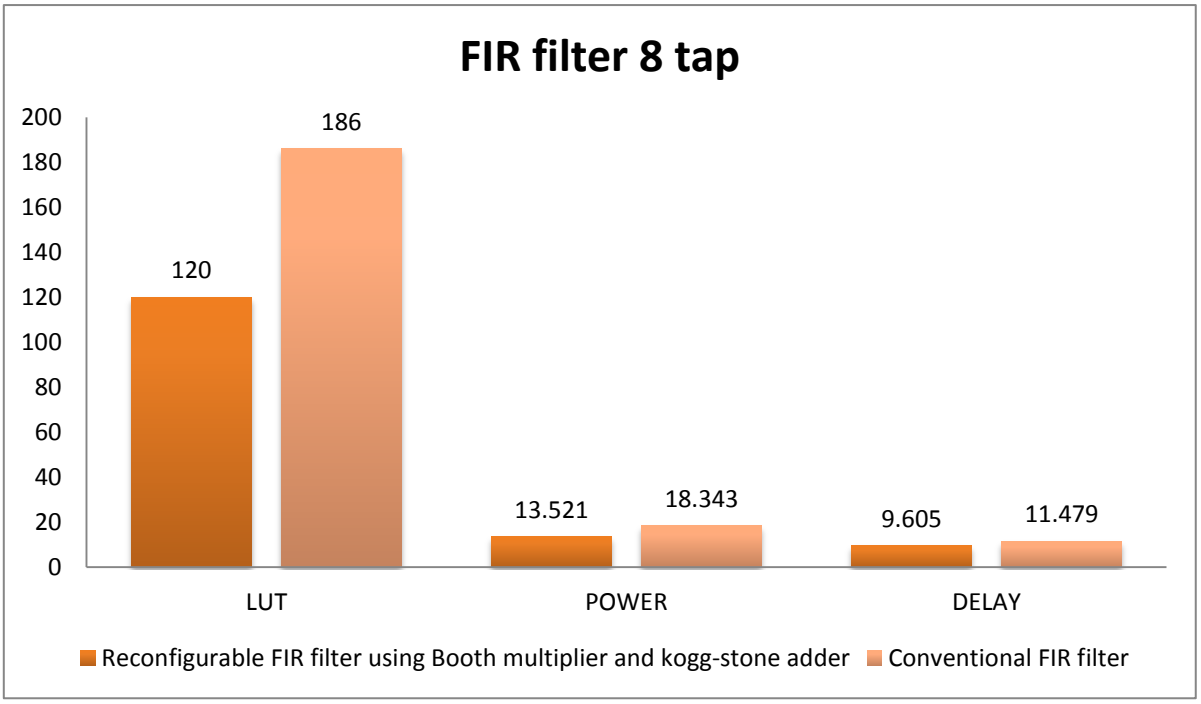

Figure 9.LUT's,power and Delay comparison of Reconfigurable FIR 8tap filter with conventional FIR filter

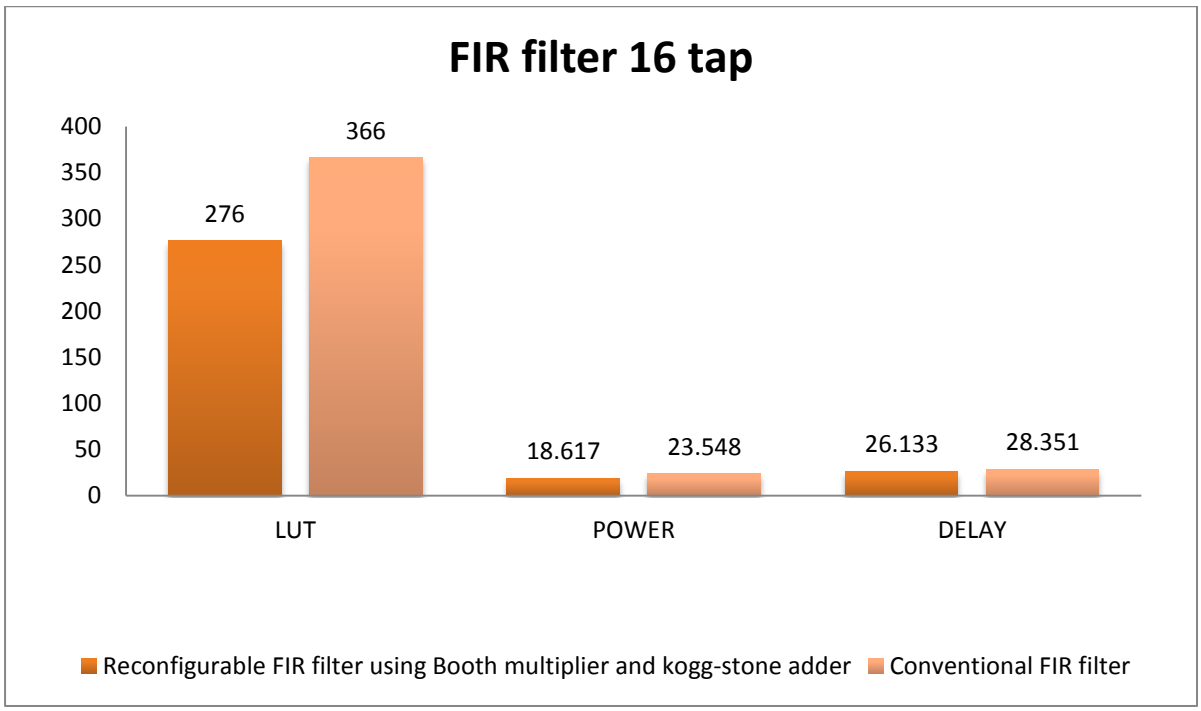

Figure 10.LUT's,power and Delay comparison of Reconfigurable FIR 16tap filter with conventional FIR filter

Conclusion

Design of Reconfigurable coefficients driven FIR filter using modified Radix-4 booth multiplier and modified kogge-stone based carry select adder is carried out in this paper .Novelty of this paper is reconfigurable coefficients in its lower LSB nibble ,Radix 4Booth multiplier using multiplexer and 2 Bit Kogge stone adder structure with and without carry using multiplexer. From the results it can be concluded that proposed Reconfigurable FIR filter design shows better performance compared to conventional FIR filter in 8 tap and 16 tap structures. The proposed design has slight decay in accuracy but it leads to best performance in LUT's, power and delay. It can be concluded that the proposed design has less area, low power consumption and also high speed in its processing inputs. Thus the proposed structure is power and area potent for VLSI applications.

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