LOW Power 7 Bit Encoder using Pseudo-Dynamic CMOS Logics

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Abstract— This paper proposed low power design 7 bit encoder. A big challenge in this designing of low power Flash ADC [4] is thermometer code (TC) to binary code (BC) converter which expands more power. Therefore an encoder which consumes low power has been implemented. Pseudo Dynamic (PD) Complementary MOS logic has been utilized for the conversion of thermometer code to the corresponding binary code since this diminishes the no. of transistors utilized. A significantly higher conversion rate can be accomplished with this encoder in correlation of conventional encoder. Sampling frequency (10GHz) can be accomplished utilizing the proposed Pseudo-Dynamic encoder. To demonstrate the performance of proposed Pseudo-Dynamic encoder, it is implemented and tested in 180 nm CMOS technology by using the Cadence tool. It exhibits that no of transistors is 504 less in correlation of 1482. The outcome unmistakably demonstrates that it is best encoder configuration style logic in terms of low power, number of Complementary Metal Oxide Semiconductors (CMOS) transistors, speed and cost.

Keywords— CMOS transistors, CMOS Inverter, AND-OR Logic. THERMOMETER CODE, GRAY CODE.

1. INTRODUCTION

The Structure of ADC consists of comparator set along the front end and a 1-out-of-N code converter for thermometer. The XOR gates are used for the implementation of the latter and is followed by encoder [4]. Each of these blocks are designed so as to achieve a circuit with high speed. Hence, this paper focuses on encoder design. Fig. 1 below shows a block diagram of typical flash type ADC.

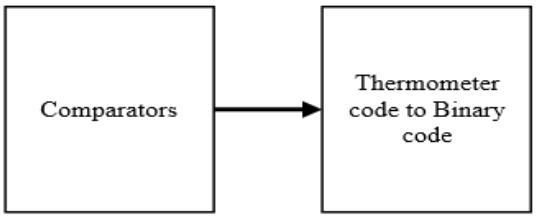


Figure.1.Block diagram of direct conversion flash ADC

Wallace tree encoder, PLA circuits/ ROM and XOR encoders are few places where the encoder is used [6]. Earlier, the Fat-tree encoder is used but as there were so many of disadvantages of this type of encoder, still it has outperformed the orthodox ROM encoder [5]. Even though there is a small scope of enhancement in this encoder, a faster and better novel encoder has been discussed which outperforms the former. The main leverage that this encoder possesses is that it can directly convert from TC to BC. Fig. 2 shows this process. A mid step of converting the thermometer code to one out of n code has now been removed. Therefore, the proposed novel encoder decreases the logic gates that has been used as a result of which power consumption has been greatly reduces and in term speed is enhanced. Thus, the proposed design is more applicable for flash ADCs which require a high speed [2].

2. DIRECT CONVERSION ENCODER USING PSEUDO-DYNAMIC CMOS LOGIC

This Encoder is designed, in similarity with PLA design utilization of just the AND-OR logic gates. The primary difference in PLA and the proposed design is that, in the former output bit is generated by combination of all the inputs. On the other hand, the present design uses only selected combination of inputs to generate the output. As already mentioned, there in no intermediate step for conversion of thermometer code into an equivalent binary code, which is its biggest advantage. The equation below mentions seven bit encoder showing the output binary bits.

Bit0=I0I1'+I2I3'+I4I5'+I6I7'+I8I9'+I10I11'+I12I13'+I14I15'
+I16I17'+I18I19'+I20I21'+I22I23'+I24I25'+I26I27'+I28I29'
+I30I31'+I32I33'+I34I35'+I36I37'+I38I39'+I40I41'+I42I43'
+I44I45'+I46I47'+I48I49'+I50I51'+I52I53'+I54I55'+I56I57'
+I58I59'+I60I61'+I62I63'+I64I65'+I66I67'+I68I69'+I70I71'
+I72I73'+I74I75'+I76I77'+I78I79'+I80I81'+I82I83'+I84I85'
+I86I87'+I88I89'+I90I91'+I92I93'+I94I95'+I96I97'+I98I99'
+II00II101'+I102I103'+I104I105'+I106I107'+I108I109'+I11
0I111'+I112I113'+I114I115'+I116I117'+I118I119'+I120I121
'+I122I123'+I124I125'+I126

Bit1=I1I3+'I5I7'+I9I11'+I13I15'+I17I19'+I21I23'+I25I27'+I
29I31'+I33I35'+I37I39'+I41I43'+I45I47'+I49I51'+I53I55'+I
57I59'+I61I63'+I65I67'+I69I71'+I73I75'+I77I79'+I81I83'+I
85I87'+I89I91'+I93I95'+I97I99'+I101I103'+I105I107'+I109I
111'+I113I115'+I117I119'+I121I123'+I125

Bit2=I3I7'+I11I15'+I19I23'+I27I31'+I35I39'+I43I47'+I51I5
5'+I59I63'+I67I71'+I75I79'+I83I87'+I91I95'+I99I103'+I107
I111'+I115I119'+I123

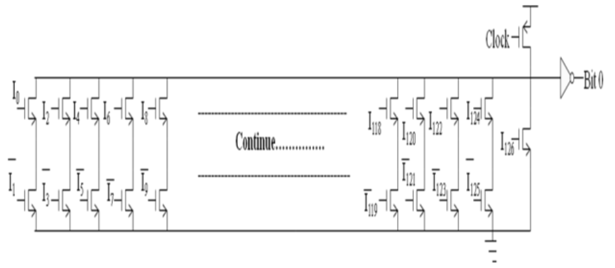
Bit3=I7I15'+I23I31'+I39I47'+I55I63'+I71I79'+I87I95'+I103
I111'+I119

Bit4= I15I31'+I47I63'+I79I95'+I111

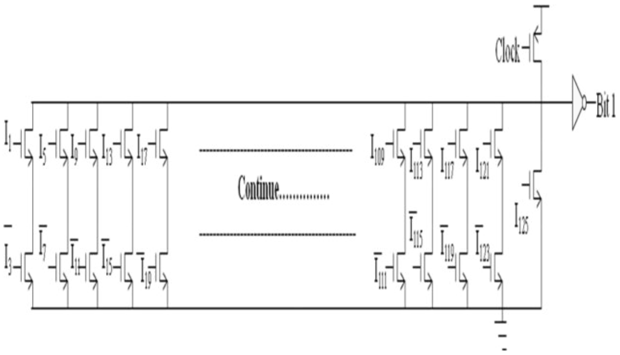
Bit5= I31I63'+I95

Bit6= I63 (1)

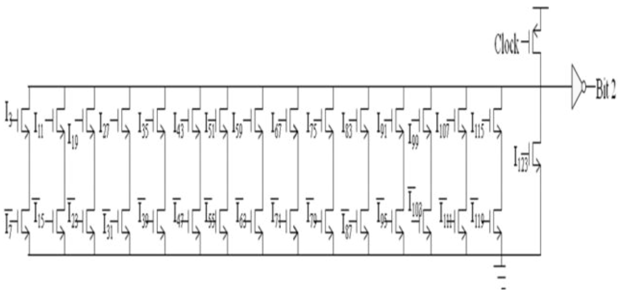
Where in the equation In stands for nth bit of thermometer code. The truth table for direct conversion encoder is shown in Table 1.



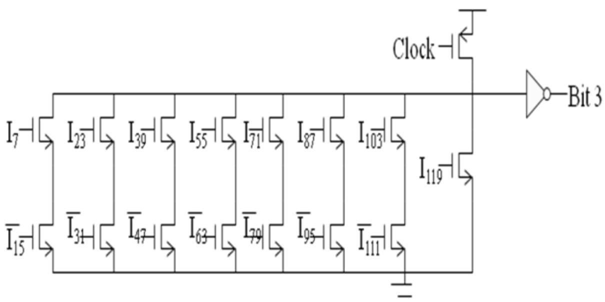
(a) Schematic for generation of Bit 0



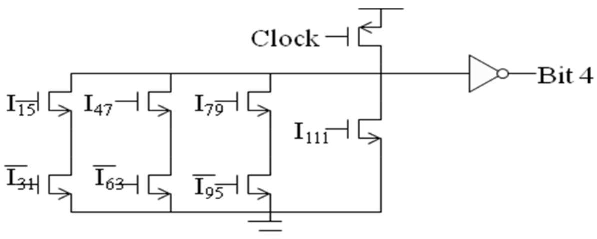
(b) Schematic for generation of Bit 1



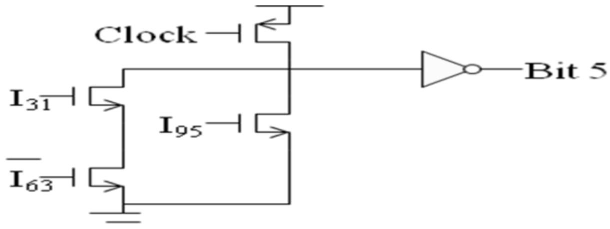
(c) Schematic for generation of Bit 2



(d) Schematic for generation of Bit 3



(e) Schematic for generation of Bit 4



(f) Schematic for generation of Bit 5

Fig.2. Encoder circuit using pseudo –dynamic CMOS logic gates

Table 1 Truth Table for Direct Conversion Encoder

Thermometer Code input I126 to I0	Encoder Output Bit6 to Bit0
0000000000000000000000000000000000000000000000000000000000000000 000000000000000000000000000000000000000000000000000000000000000	0000000
0000000000000000000000000000000000000000000000000000000000000000 000000000000000000000000000000000000000000000000000000000000001	0000001
0000000000000000000000000000000000000000000000000000000000000000 000000000000000000000000000000000000000000000000000000000000011	0000010
0000000000000000000000000000000000000000000000000000000000000000 000000000000000000000000000000000000000000000000000000000000111	0000011
0000000000000000000000000000000000000000000000000000000000000000 000000000000000000000000000000000000000000000000000000000001111	0000100
CONTINUE... ... ... - .... -	CONTINUE..... - -- ------ ------
1111111111111111111111111111111111111111111111111111111111111111 111111111111111111111111111111111111111111111111111111111111111	1111111

According to the equation (1), the bits at the output are determined straight from the comparator output to the TC (Thermometer Code). The significance of this that the "0-1" circuit generator is eliminated thereby is reducing the encoder delay by some margin. The equations are derived from truth table for this Encoder. Bits having the same entries are equated, for example Bit-3 of the output is equated with the Bit-I7 of the input. Thus, there is no need for any intermediate processing step and can be directly used to drive the output. In the similar manner equation for also derived by matching the

bit pattern. These results in realizing these equations by using less NMOS gates compared to its predecessors.

This circuit can be designed using different techniques such as pseudo N-MOS, Static (S) CMOS or Dynamic (D) CMOS logic. S-CMOS logic can give low power dissipation but at the same time they are unable to provide a high speed. D-CMOS logic on the other hand can achieve a high speed but at the cost of high power dissipation. Therefore, the Pseudo Dynamic design CMOS logic is used to implement the proposed architecture which includes a new CMOS logic. This logic implementation requires a PMOS transistor, coupled with a few NMOS transistor and an inverter to complete it. The purpose of PMOS here is to work like pre charge circuit for for the output node on one hand and/or to achieve a peak value. NMOS on the other hand are used for the purpose of achieving the lowest value. On contrary to the D-CMOS logic, NMOS evaluation interpretation transistors and not required with NMOS logic block in as the input to this circuit are provided by outputs from flash ADC's comparators which are clocked and these can latch the output till the next rising edge of clock.

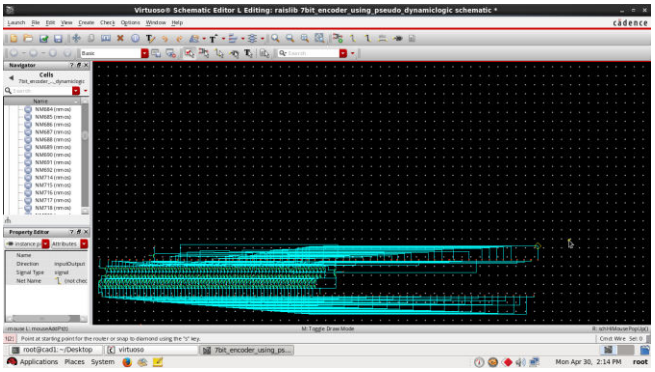
Another point to focus here is that, for D-CMOS logic, during the precharge phase it is important that NMOS circuit is disabled. Whereas for the pseudo dynamic CMOS logic, it is not of consideration as NMOS logic has no effect on the voltage level of output. Thus happens because of the presence of inverter. If during the precharge phase, NMOS logic is enabled, then the intermediate voltage of resistive divider created by the pull up and NMOS logic determines the output level.

The important point to focus here is that the input voltage of the inverter should not be above the V_{IH} level, which denotes the maximum value of input voltage of inverter which is considered as logic zero level. This is achievable if the size (width) of both the NMOS and PMOS of the inverter are selected carefully, else an undesirable output will be provided by the circuit [3]. Take an example, the clock is low and the NMOS logic has been enabled. If the size (width) of both the transistors are carefully selected, then input voltage to the inverter will be lower that the designate V_{IH} value at the output. There is one disadvantage of this proposed CMOS logic, which is that this logic does not provide a non zero static power dissipation, It is caused by current that is passing through the pull down network during the low transition of the clock.

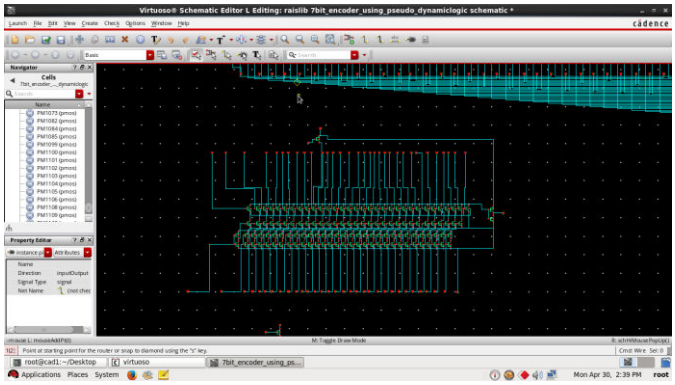
Fig. 3 shows the AND-OR gate implementation using the proposed Pseudo-Dynamic CMOS logic. The circuit consists of clock driven PMOS transistor along with a block of NMOS logic which defines the logic functioning. Inputs that are to be ORed in NMOS logic are connected in parallel branches and the ones that are to be ANDed are connected in series.

3. SIMULATION SETUP

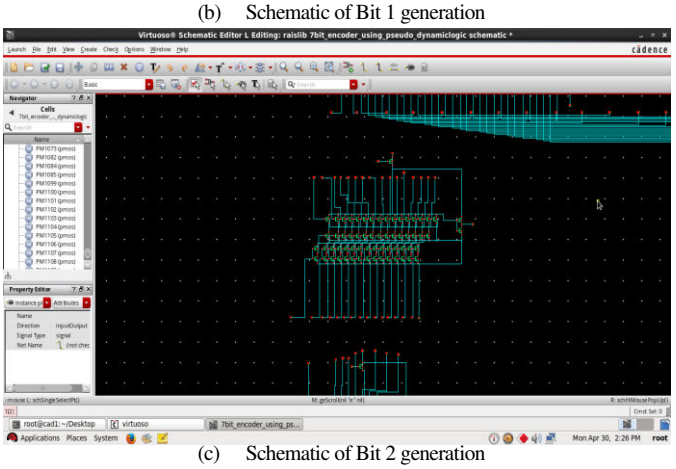
7 Bit encoder using the Pseudo-Dynamic CMOS logic has been Design in Cadence Tool in 180nm CMOS Technology. We have observed that the minimum number of transistors is using in comparison of fat tree encoder.



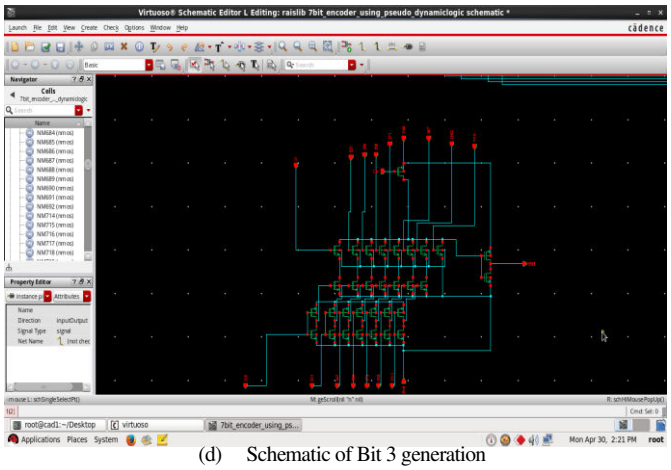
(a) Schematic of Bit 0 Generation



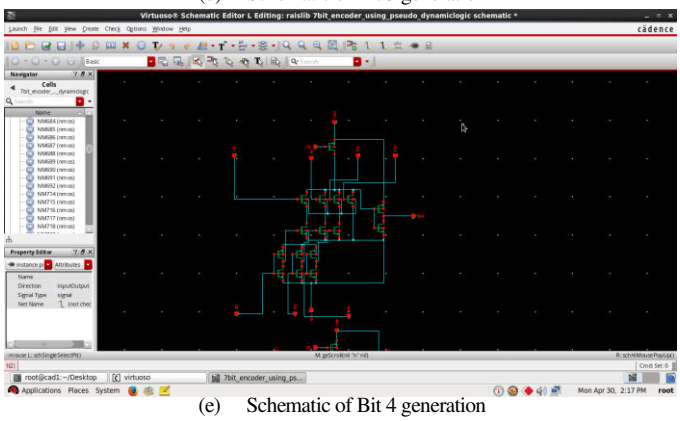
(b) Schematic of Bit 1 generation



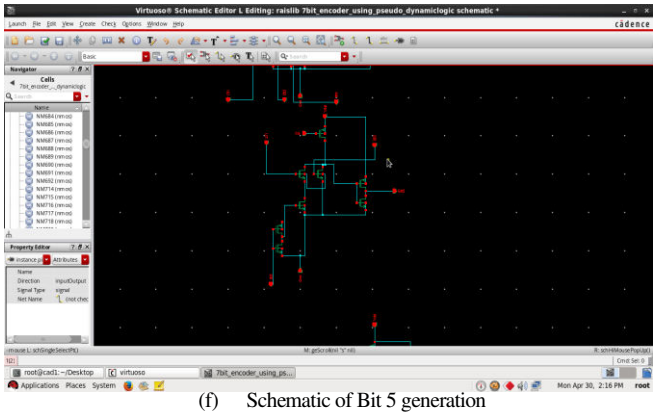
(c) Schematic of Bit 2 generation



(d) Schematic of Bit 3 generation



(e) Schematic of Bit 4 generation



(f) Schematic of Bit 5 generation

Fig.3. Schematic of encoder using pseudo-dynamic logic gates

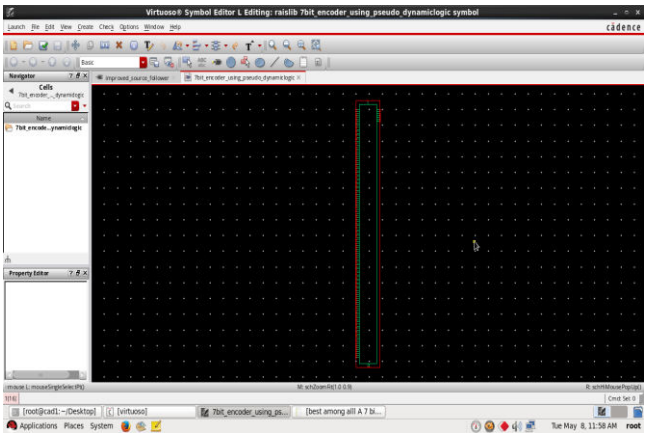


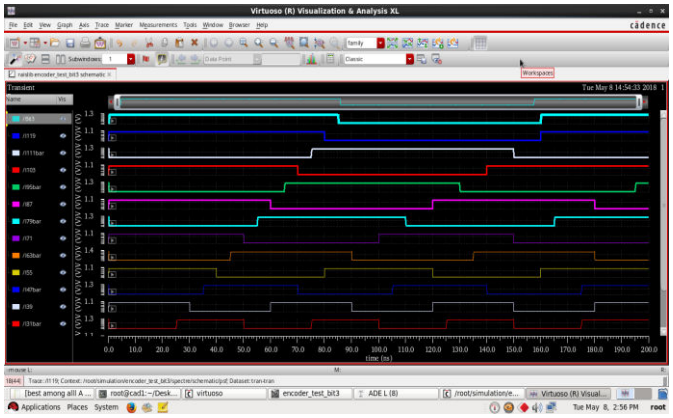
Fig.4.Symbol of Direct conversion encoder using pseudo- dynamic CMOS logic.

4. TRANSFER CHARACTERISTIC OF ENCODER USING PSEUDO-DYNAMIC AND-OR LOGIC

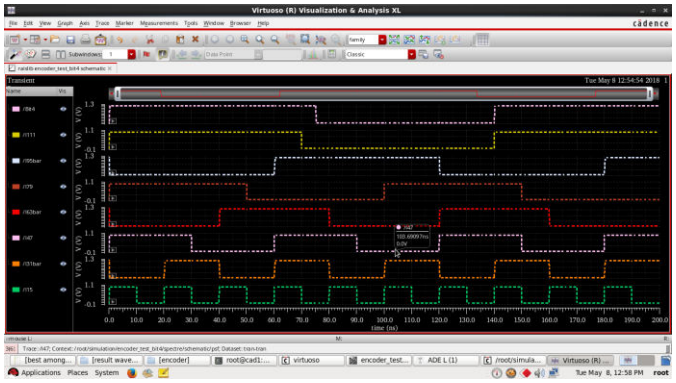
7 Bit encoder has implemented and tested in Cadence tool. The transfer characteristic has been plotted. Therefore number of transistor has been reduced by using the Pseudo-Dynamic CMOS logic. In Fat tree encoder, for 7 bit 1482 MOS transistors can be used but in direct conversion Pseudo-Dynamic CMOS logic only 504 MOS transistors is required as shown in table 2. We have been observed less power dissipation is consumed in comparison of fat tree encoder.

Table 2 Table for Comparison of CMOS transistors

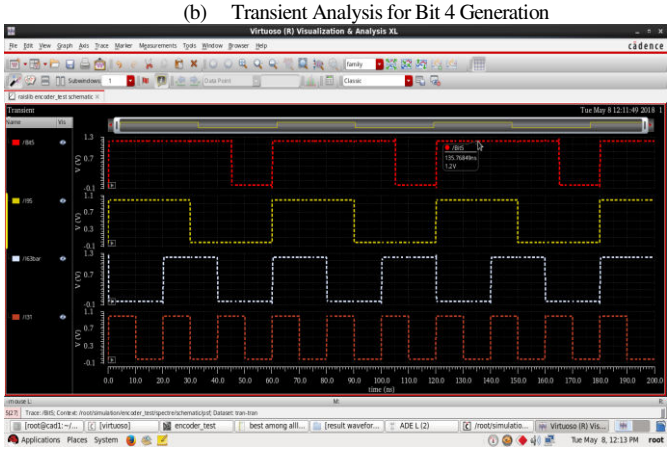
LOGIC Style	Number of MOS transistors
Fat tree Encoder	1482
Direct Conversion using Pseudo-Dynamic Encoder	504



(a) Transient Analysis for Bit 3 Generation



(b) Transient Analysis for Bit 4 Generation



(c) Transient Analysis for Bit 5 Generation

Fig.5. Transfer characteristic of 7 bit encoder using the Pseudo-Dynamic CMOS logic.

5. CONCLUSION

We have design and simulate the low power 7bit encoder using the Pseudo-Dynamic CMOS logic. Thereafter this paper has compared with fat tree encoder in terms of no MOS transistors and power dissipation. We have seen the performance is better than other encoder. Along with this we have implemented the Flash ADC the circuit has been simulated and the corresponding transient response has been analyzed.

6. REFERENCES

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