A Multiple Threshold Driver LRFF for Low Power Applications

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Abstract: In this paper, a multiple threshold driver LRFF is presented which is intended for low power applications. The design contains a master slave configuration with 19 transistors. A method of multi-V_t technique is employed in the circuit to attain low power. As the semiconductor technology is progressing deeply in to the sub-micron geometries of below 100 nm, the technology is required to fabricate the composite SOC designs needed for today's portable devices like mobile phones, laptops and many others. In deep sub-micron designs, the balance between chip performance and power is becoming gradually an important issue. Accordingly, a method of Mixed Multi-V_t approach is utilized in the circuit's critical region. Thus, balance between both power and performance of the circuit is also achieved. This entire analysis is done by using 45nm technology.

Keywords: Cadence virtuoso 6.1, flip flops

I. Introduction:

For the time being, the power utilization has prominent in integrated circuits and systems design. In 90's era the significant works of VLSI design engineers were high speed, less area and low cost, but the problem of low power somehow got less concern. Though, the evolution of personal computing devices and wireless computing systems has enforced designers to explore low power techniques [1]–[9] with high reliability. With the difficulty of heat dissipation the portable and hand held products would present low battery life without the utilization of low power design methodologies. Moreover, reliability is greatly influenced by power consumption. Besides this, high power dissipation signifies high temperature operation, which leads to the numerous failures in the system. Thus, power becomes a significant concern in the today's VLSI designs.

Over the past decade the main technological advancements to attain low power region have been affiliated with the portable electronic devices. To design synchronous VLSI digital systems the essential components are Flip-Flops and latches. The maximum working speed of clocked digital systems is determined by Flip-Flops. In the view of to attain low power design, Flip-Flops and the clock distribution network both dissipates approximately 30-70% of total chip power [11].Consequently, for digital IC designers reduction of clock power is an important task. To cut down the clock load and related power dissipation in the clocking network numerous efforts found to be published in the past. Moreover, the design occupies more area because of high transistor count. Because of that reason the overall manufacturing price of the chip increases. Specific application like high speed, low power and low voltage call new Flip-Flop designs [12]-[15]. Therefore, interns of advanced speed, reduced power dissipation and less transistor count it has always been a challenge to explore more effective FF designs.

Flip-Flops are basic memory elements used enormously in the design of digital system. A digital system is made up of gates along with flip flops that are bind together. Hence, the soul of the design method is to identify exactly what gates and flip flops should be used.

Depending on the nature of application Flip-Flops are generally classified in to four major categories. They are as follows

- Master-Slave FFs
- Pulse triggered FFs (implicit pulse triggered and explicit pulse triggered)
- Differential Flip – flops
- Dual edge triggered Flip – flops

Master – slave Flip flops are commonly utilized for low power applications while pulse triggered FFs utilized in high speed applications. For intensely pipelined systems, differential FFs are used where the flip-flops have to furnish complementary output

signals to the consequent logic. Concurrently, DETFF (Dual edge triggered Flip-Flop) is utilized for supporting a stable output when operating at half the clock frequency. In this paper, a Multiple Threshold Driver LRFF is designed with master slave configuration for low power applications.

This paper is structured as follows. In section II literature survey of this work is presented. The summary of some existing FFs is presented in section III. In section IV, the proposed design and its working is presented. The experimental results are shown in section V. In section VI the conclusions are given.

II. Literature survey

Anantha P. Chandrakasan et al. [1] have presented the techniques to accomplish the low power consumption in CMOS digital circuits.

A MTCMOS technology is furnished by shin'ichiro mutoh et al. [2]. In this technique the MOSFET's utilizes two different threshold voltages.

Naran sirisantana et al. [3] have demonstrated two novel techniques M_LCMOS and M_{OX}CMOS to attain low power and upgrade of CMOS circuits.

For battery operated portable devices, the idea of utilizing Multi threshold CMOS is presented by Satoshi Shigemastu et al. [4].

Liqiong Wei et al. [5] have presented a dual threshold technique to cut the leakage power. In this technique, in non critical paths high threshold voltage transistors are assigned, and in critical paths low threshold transistors are assigned.

Ram K. Krishnamurthy et al. [6] have conflicts for sub-70nm microprocessor circuits. In this work, he considered the new design disputes for high speed and low power microprocessors.

Minimizing power under performance constraint is presented by Ruchir puri et al. [7]. In his work, he analyzes the balance involving in both the multiple supply voltages and multiple threshold voltages in the optimization of dynamic and static power.

Frank Sill et al. [8] have proposed a reducing leakage with mixed-Vth (MVT). In his work, he furnishes a new scheme in a double V_{th} procedure for obligation of devices with different V_{th}.

Amit Agarwal et al. [9] have studied the effectiveness of dual Vt designs under combative scaling of technology. To understand high speed and low leakage dual-Vt designs in sub-50nm metal gate work functions progression options are required.

The influence on the buffer circuit by Short-circuit power dissipation of static CMOS circuitry is demonstrated by Harry J.M. Veendrick et al. [10]. On the base of an elementary CMOS inverter, the short circuit component in the total power dissipation of CMOS circuits is discussed in this work.

Hiroshi Kawaguchi et al. [11] have presented a RCSFF. He furnished a novel small-swing clocking scheme to obtain low power.

Masataka Matsui et al. [12] have proposed a SAFF scheme which is utilized in a 200 MHz 13mm^2 2-D DCT Macro cell. By using this scheme the speed of the propagation of the signal is increases and area is reduced. It is used in applications like carry skip adder which is used in DCT MAC's to shortens the propagation delay and reduce the macro cell size.

B.Nikolic et al. [13] have proposed an Improved sense-amplifier based flip-flop: Design and measurement. In his work he introduced a new SAFF. In the advanced processors it is placed as the fastest flip flops demonstrated by its speed.

Vladimir Stojanovic et al. in [14] have presented the regulations for the assessment of speed and power features of the FF and master - slave latches.

Hamid partovi et al. [15] have demonstrated the timing methodology of HLFF intended at a substantial deduction in latch latency and clock load is described by his work.

To reduce the pipeline overhead semi dynamic and dynamic FFs with embedded logic are presented by Fabian Klass et al. [16].The application of this design is in used in microprocessor design for high performance.

James Tschanz et al. [17] have presented a pulsed flip-flops to provide an excellent method of delay and energy requirements to alleviate clock skew effects while contributing time borrowing ability.

To attain statistical deduction of power Bai – sun kong et ai. [18] have presented a conditional capture flip flop. The low power is obtained by redundant transitions.

The conditional discharge flip flop is presented by Peiyi Zhao et al. [19] for high speed and low

power. In this work conditional pre charge technique and conditional capture technique are presented to avoid the redundant switching activities.

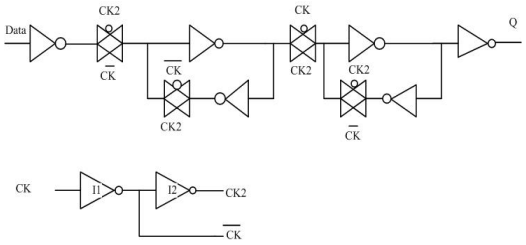
Myint Wai Phyu et al. [20] have presented two flip flops DET-SAFF and CGSAFF to attain Low power and high speed aspects. This is obtained by utilizing dual edge triggering mechanism and conditional pre charging.

Chen Kong tech et al.[21] have designed an ACFF which is a D flip flop in 40-nm CMOS. This ACFF has 22 transistors and it is more energy efficient than TGFF.

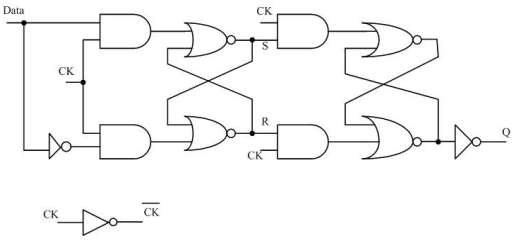
Natsumi Kawai et al. [22] have presented a TCFF with 21 transistors. The ratio of power deduction using TCFF is greater compared to other low power FFs. It is achieved by using topological compression methodology that is merger of logically equivalent transistors.

III. Summary of existing FF designs

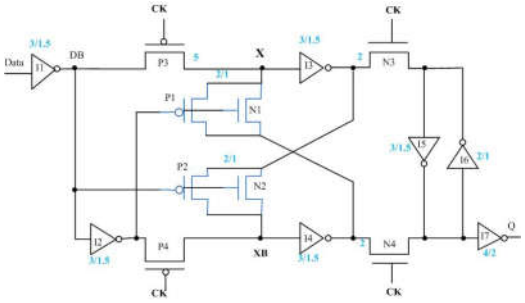
To provide comparisons we are studied some basic existing FFs. They are TGFF, SRFF, ACFF and TCFF shown in fig1.(a), 1(b), 1(c) and 1(d) respectively. At present the mostly used flip-flop is the TGFF but it has the disadvantage of excessive clock load due to that a large power consumption takes place. The SRFF also suffer with the same problem as that of TGFF. To overcome this ACFF[21] and TCFF [22] are designed. As a result of data contention problem of ACFF, the advantage of power consumption in ACFF is ignored. In TCFF also due to the expansion of the PMOS transistors the power consumption is influenced.



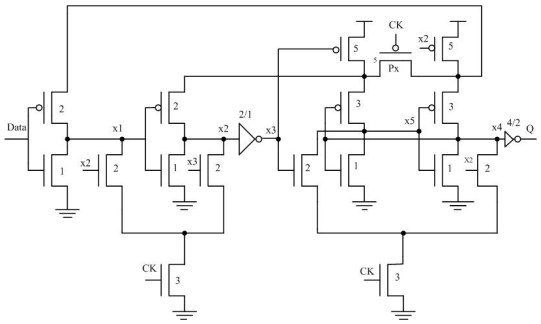
1.(a) TGFF



1.(b)SRFF



1.(c) ACFF



1.(d) TCFF

IV. Proposed Circuit

The proposed Multiple threshold driver LRFF employed a mixed multi-v_t technique to achieve low power and high-performance aspects. The circuit diagram of Multiple Threshold Driver LRFF is shown in fig.2.

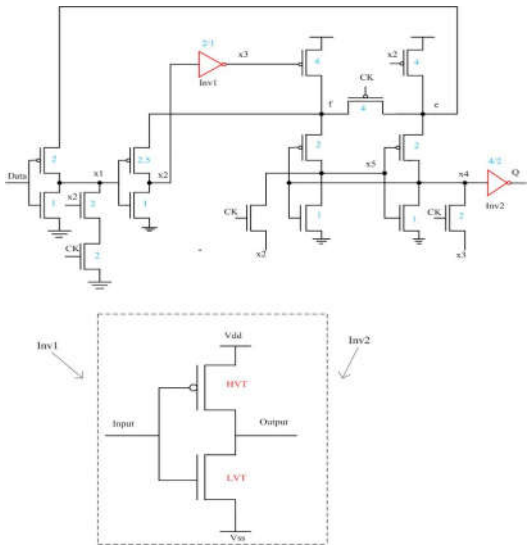


Fig.2. Multiple Threshold Driver LRFF

The Multiple threshold driver LRFF contains a master-slave configuration with 19 transistors. A master-slave FF can perform an essential task in functioning critical operations of successive stages of digital circuits. The driving circuit [10] will take a comparatively large part of the total power consumption and it also takes more delay. By reducing the power consumption and delay at this driver part (critical part), we can achieve the complete circuit power and speed aspects. To achieve this, a method of mixed multi-V_t approach is applied in the critical (driver) part of the design. Thus, we can reduce the circuit power and delay as well.

Mixed Multi-V_t technology:

Generally, the current invention relates to cell-based design by using deep sub-micron devices. Yet more especially, the present revelation associate with the technique of integrating mixed multi-V_t devices in DSM standard cells. Consequently, increasing in speed and reducing power dissipation can be attained. With the scaling of multi-Vt devices to transistor level, a cell-based design can meet up the speed and power performance of a full custom design rather than cell level.

To combine more complicated functionality at superior performance on a single chip semiconductor technology is progressing into the very deep sub-micron geometries of less than 100 nm. This technology is required to fabricate the compound SOC designs needed for today's portable devices like laptops, mobile phones, and other electronic gadgets. Because these portable devices utilize batteries hence the chip power dissipation has become a crucial factor as circuit performance.

Sub-100 nm devices give more complicated functionality and higher performance, but the cost is high. It has been noticed that, when the channel length of the transistor is small the current continues to flow because of leakage. For this reason, power is uselessly dissipated in these nanometer regions. Consequently, the battery power is drained. In DSM technology the balance between speed and power of the circuit is becoming gradually an important issue.

To resist this problem, manufacturers have fabricated sub-100 nm devices with high-Vt. But these HVT devices are slow and can affect the chip speed and performance. Due to the less speed of the high-Vt devices the circuit performance may not meet its requirements yet. To meet up both speed and power constraints in sub-100 nm designs a balance between speed and power dissipation must be created.

Generally circuits are designed by using circuit cells. Circuit cells are basic building blocks that have all transistors included inside with the similar transistor properties. The transistors in a cell are either all HVT devices or all LVT devices. To accommodate devices with different threshold properties there is no standard cell available to maximize the functions of the cell.

Mostly LVT devices are utilized for a speed-critical design, and HVT devices are used in a power-critical design. The method of mixed low-Vt and high-Vt devices are useful in the art of cell design. Thereby a balance between both speed and power criteria may be performed and optimized.

Working:

The working of Multiple threshold driver LRFF is shown in fig. 3(a), 3(b), 3(c) and 3(d) respectively.

D=0 & CK=0

When d=0 and ck=0, the master latch goes to transparent state. The node x_2 is driven to zero and node x_3 is driven to one. The transistors n_7 and n_{10} are clock controlled feed-in transistors. When n_7 and n_{10} are turned off signals are blocked which are coming from the master latch from entering the slave latch. The slave latch is now going to hold state and the output keeps not changed. Note that x_2 fed to p_3 and x_3 fed to p_5 of the slave latch are not meant for signal input. Rather, they help to control the pseudo V_{DD} nodes e and f. The nodes e and f are bridged by p_x

which is controlled by clock and ensuring that they both become $V_{DD.}$

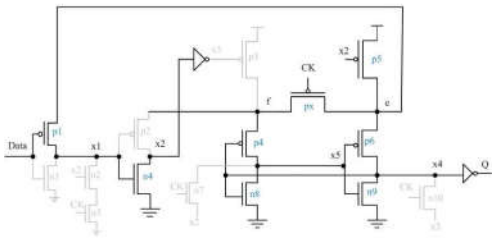


Fig. 3(a) D=0&CK=0

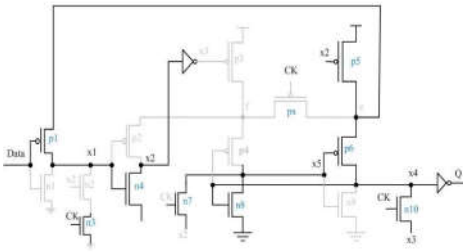


Fig. 3(b) D=0&CK=1

D=0 & CK=1:

When D=0 and CK=1 the data i.e., x_2 and x_3 enters in to the slave latch from the master latch via the transistors n_7 and n_{10} respectively. The state of the slave latch is changed by maintaining the values of node x_2 and x_3 for a sufficient amount of time. Since the transistor p_x which is controlled by clock currently turned off, a fast state transition is facilitated by disconnecting node 'f' from $V_{DD.}$ The transistors p_2 and n_4 are turned off after the hold time when the input data change. In this way the data is blocked from the master latch entering to the slave latch. Through the pass transistor n_7 a reverse signal is flowing, so that the node x2 is stays at 0. Hence, there is no internal node floating problems occur.

D=1 & CK=0:

When D=1 and CK=0, for to admit the new data the master latch is transparent state and the slave latch is in hold state. Transistor p_3 is turned ON for the slave latch and V_{DD} is passed to the node "e" from the node "f" with the help of bridge transistor p_x.

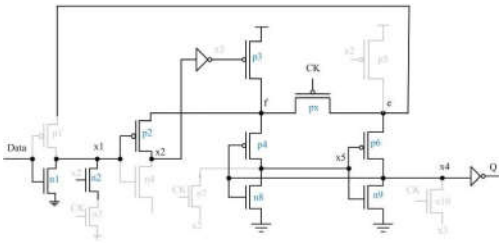


Fig. 3(c) D=1&CK=0

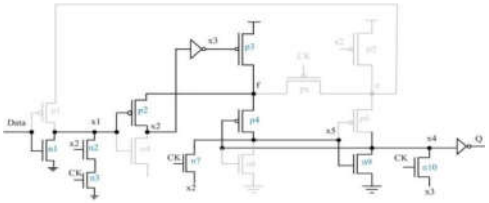


Fig. 3(d) D=1 & CK=1

D=1 & CK=1:

When D=1 and CK=1, the master latch is in hold state and the value of slave latch changes accordingly. The slave latch state transition is speed up by the transistor p_5 controlled by x_2 is turned off. Due to the shutdown of the V_{DD} path of the incoming stage inverter after the hold time any signal changes cannot even enter the master latch.

Simulation wave forms at 50 KHz/1 V are shown in fig.4.

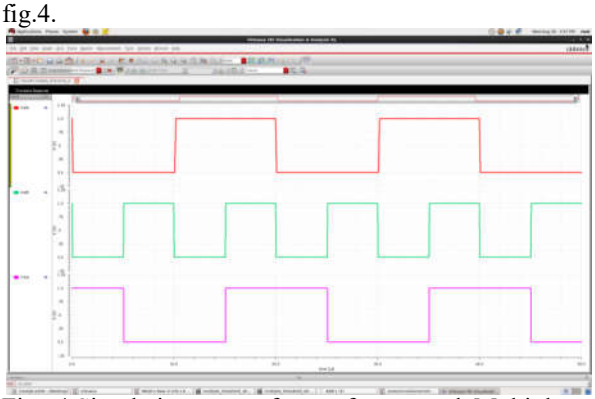


Fig: 4.Simulation wave form of proposed Multiple Threshold Driver LRFF

V. Simulation Results

Various FF designs were enclosed in the simulations for performance assessment. They are TGFF, SRFF, ACFF, TCFF, LRFF and the proposed

Multiple threshold driver LRFF. The analysis involved in three categories. The first category is power consumption, the second one is delay (DQ and CQ) and the third one is area which contains transistor count and layout area. The nominal working condition was 50 KHz/ 1V/ TT-Corner. The designs may function properly at other frequencies also. The simulation and evaluation results are outlined in Table 1.

FF DESIGN	TGFF	SRFF	ACFF	TCFF	Multiple threshold driver LRFF
No.of transistors	24	30	22	21	19
Area($\mu m^{2)}$	25.58	33.63	25.52	26.37	19.31
D to Q delay	5.040	5.040	5.04	25.03	5.026
CK to Q delay	5.060	5.060	5.068	25.05	5.051
Power(nW)	12.89	30.89	45.88	2.521	2.419

Table 1: Comparison results of various FF designs at 50 KHz/1V/TT-Corner

A. Power consumption analysis:
Compared to the other existing FF designs the proposed design is efficient. The comparison results are shown in fig.5.

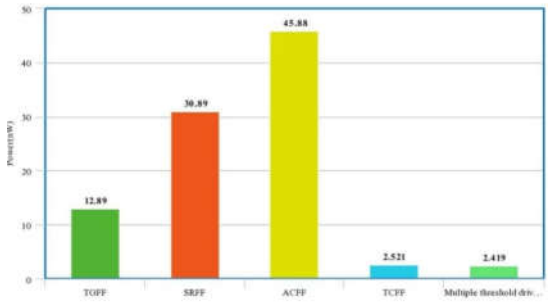


Fig.5. Power consumption analysis of various FFs

B. Delay analysis:
The proposed design is effective compared to all other flip flop designs in terms of D to Q delay and C to Q delay. The comparison result is shown in fig.6 and fig.7.

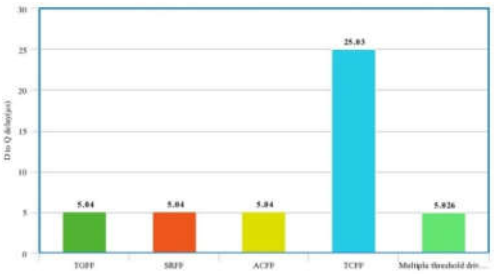


Fig.6. D to Q delay

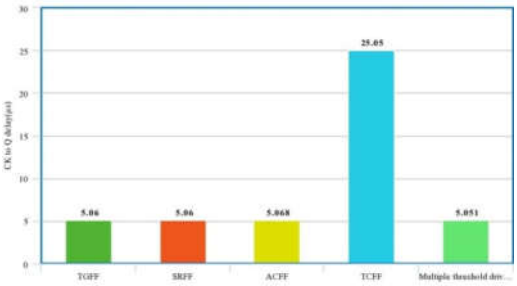


Fig.7. C to Q delay

C. Area analysis:
The proposed Multiple threshold driver LRFF employs the less transistor count and attributes the smallest area. The layout size of proposed design was measured as 5.565 µm × 3.47 µm. The area comparison of various FF designs is shown in fig.8 and the layout of proposed design is shown in fig.9.

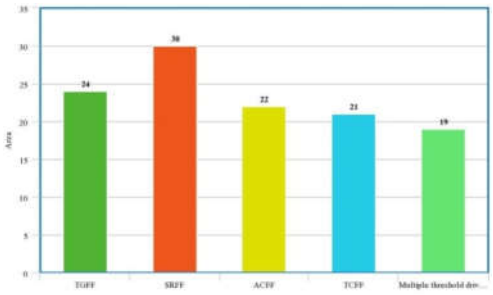


Fig.8. Area of FFs

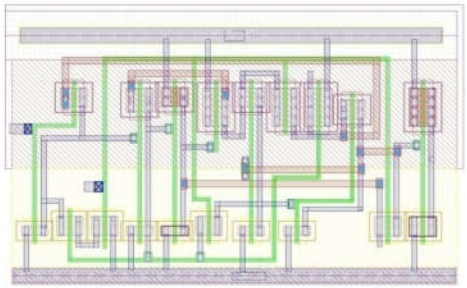


Fig.9. Layout of Multiple threshold driver LRFF

VI. Conclusion

In this paper, we present a Multiple threshold driver LRFF by employing a mixed multi-V_t technique for low power and high speed applications. The circuit utilizes the master-slave configuration with 19 transistors which is identical to the LRFF. The key idea is applying a mixed multi-V_t technique in the critical region of the design which plays an important role for complete analysis of the circuit. The simulations were conducted on various FF designs and performance analysis was taken. The proposed circuit got efficient results compared to other designs. Thus, the proposed circuit is the efficient one.

VII. Future scope

The main drawback in using this Mutli-V_t technique is that the design complexity is increases even though we are achieving a trade-off between both circuit speed and power. So, to fix this issue we have to apply the suitable technique to reduce the design complexity to achieve both the power and speed analysis.

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